TPS65951

Integrated Power Management/Audio Codec

Silicon Revision 1.0

Version F

Data Manual

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Literature Number: SWCS053F
September 2010–Revised May 2012

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Integrated Power Management/Audio Codec

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1 Introduction

The TPS65951 device is a power-management IC for mobile cellular handsets powered by a Li-ion, Li-ion polymer, or cobalt-nickel-manganese cell battery. It can be connected to an application processor and/or a modem. This optimized power-management IC is designed to support the specific power requirements of the OMAP processor devices. The TPS65951 contains several buck converters, low dropout (LDO) regulators, battery charger interface, and a host of other features and functions. The audio portion of the TPS65951 is an entire audio module with audio codecs, digital filters, input preamplifiers/amplifiers, and class D output amplifiers.

This TPS65951 Data Manual presents the electrical and mechanical specifications for the TPS65951 device. It covers the following topics:

- A description of the TPS65951 terminals: assignment, multiplexing, electrical characteristics, and functional description (see Section 2)
- A presentation of the electrical characteristic requirements: maximum and recommended operating conditions, digital I/O characteristics (see Section 3)
- The clock specifications: clock slicer, input and output clocks (see Section 4)
- The audio/voice module with the electrical characteristics and the application schematics for the downlink and uplink path (see Section 5)
- The power module including the power provider, power references, power control, the power consumption, and the power management with the sequence on and off (see Section 6)
- The timing requirements and switching characteristics (ac timings) of the interfaces (see Section 7)
- The battery charger interface (see Section 8)
- A description of different modules: MADC and LED drivers (see Section 9 and Section 10)
- The deboucing time (see Section 11)
- A description of the external components for the application schematics (see Section 12)
- The thermal resistance characteristics, device nomenclature, and mechanical data about the available packaging (see Section 13)
- A glossary of acronyms and abbreviations used in this data manual (see Section 14)

1.1 TPS65951 Block Diagram

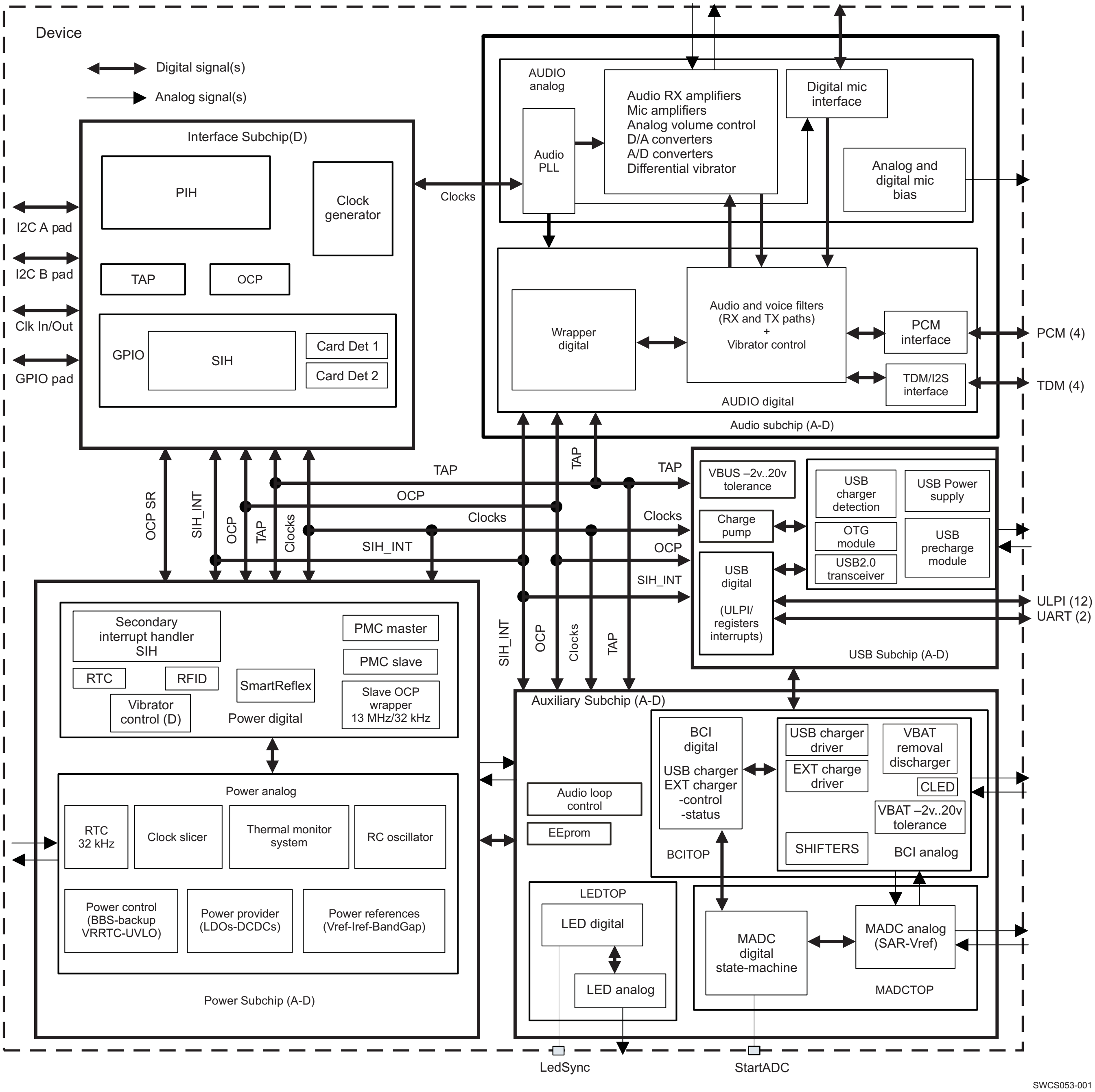


Figure 1-1. TPS65951 Block Diagram

2 Terminal Description

Figure 2-1 illustrates the ball locations for the 169-ball plastic ball grid array (PBGA) package and is used in conjunction with Table 2-1 to locate signal names and ball grid numbers.

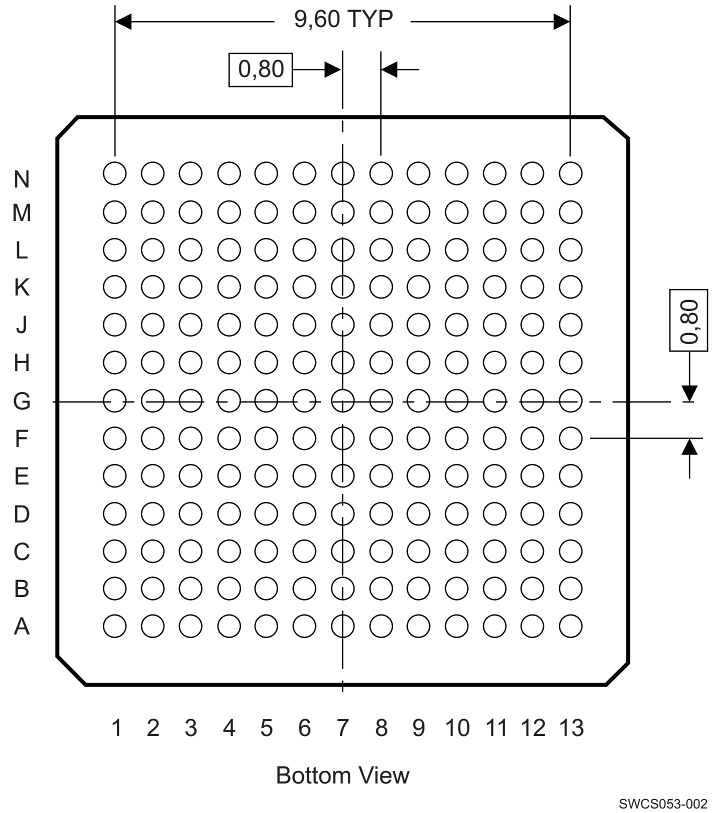


Figure 2-1. PBGA Bottom View

2.1 Corner Balls

The four corner balls (TEST, TESTV1, TEST.RESET, and TESTV2) are not useable for functional pins.

2.2 Ball Characteristics

Table 2-1 describes the terminal characteristics and the signals multiplexed on each pin. The following list describes the table column headers:

1. **BALL:** ball number(s) associated with each signal(s)
2. **PIN NAME:** the names of all the signals that are multiplexed on each ball
3. **A/D:** analog or digital signal
4. **TYPE:** the terminal type when a particular signal is multiplexed on the terminal
5. **REFERENCE LEVEL:** the voltage applied to the I/O cell (see Section 6 and Section 8 for values).
6. **PU/PD:** denotes the presence of an internal pullup or pulldown. Pullups and pulldowns can be enabled or disabled via software.
7. **BUFFER STRENGTH:** drive strength of the associated output buffer
8. **ESD RAIL:** power reference for ESD protection

Table 2-1. Ball Characteristics

BALL [1]	PIN NAME[2]	A/D [3]	TYPE [4]	ESD RAIL[8](3) VDD	REFERENCE LEVEL RL[5]	PU[6] (kΩ)(4)			PD[6] (kΩ)(4)			BUFFER STRENGTH (mA)[7]
						MIN	TYP	MAX	MIN	TYP	MAX	
K1	ADCIN0	A	I/O	ADCIN0	VINTANA1.OUT							
G3	ADCIN1	A	I/O	None	VINTANA1.OUT							
F4	ADCIN2	A	I	VINTANA2.OUT	VINTANA2.OUT							
J5	USBCHRG_ENZ	A	O	VPRECH	VPRECH							4
H5	USBCHRG_STATZ	A	I	VPRECH	VPRECH	65		139				
K4	VPROG	A	I	None	VPP							
L1	VPRECH	A	O	None	VPRECH							
K6	CHRG_DET_N	A	O	VPRECH	VPRECH							4
K12	VREFGND	A	Power GND	None	GND							
L5	VBAT	A	Power	AGND	VBAT							
M8	GPIO.0/CD1	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	8
	JTAG.TDO	D	I/O	IO.1P8	IO.1P8							8
L9	GPIO.1/CD2	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	2
	JTAG.TMS	D	I	IO.1P8	IO.1P8							
J3	GPIO.2	D	I/O	IO.1P8	IO.1P8	156	220	450	59	100	144	2
	TEST1	D	I/O	IO.1P8	IO.1P8							2
L10	GPIO.15	D	I/O	IO.1P8	IO.1P8	156	220	450	59	100	144	2
	TEST2	D	I/O	IO.1P8	IO.1P8							2
K3	GPIO.6	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	2
	PWM0	D	O	IO.1P8	IO.1P8							4
	TEST3	D	I/O	IO.1P8	IO.1P8							2
	CLKOK											
M13	GPIO.7	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	2
	VIBRA.SYNC	D	I	IO.1P8	IO.1P8							
	PWM1	D	O	IO.1P8	IO.1P8							4
	TEST4	D	I/O	IO.1P8	IO.1P8							2
L11	START.ADC	D	I	IO.1P8	IO.1P8							
E8	SYSEN	D	Open drain/I	IO.1P8	IO.1P8	4.7	7.35	10				2
F6	CLKEN	D	O	IO.1P8	IO.1P8							2

Table 2-1. Ball Characteristics (continued)

BALL [1]	PIN NAME[2]	A/D [3]	TYPE [4]	ESD RAIL[8][3] VDD	REFERENCE LEVEL RL[5]	PU[6] (kΩ)[4]			PD[6] (kΩ)[4]			BUFFER STRENGTH (mA)[7]
						MIN	TYP	MAX	MIN	TYP	MAX	
B13	CLKREQ	D	I	IO.1P8	IO.1P8				60	100	146	
B10	INT1	D	O	IO.1P8	IO.1P8							2
C10	NRESPWRON	D	O	IO.1P8	IO.1P8							2
A11	NRESWARM	D	I	IO.1P8	IO.1P8							2
F7	PWRON	D	I	VBAT.RIGHT	VBAT							
C11	NSLEEP1	D	I	IO.1P8	IO.1P8							
J13	BOOT0	A/D	I/O	VPLLA3R.IN	VBAT							
G10	BOOT1	A/D	I/O	VPLLA3R.IN	VBAT							
D8	REGEN	D	Open Drain	VBAT.LEFT	VBAT	5.5	8	12				2
B7	MSECURE	D	I	IO.1P8	IO.1P8							
K13	VREF	A	Power	None	VREF							
G7	AGND	A	Power GND	None	GND							
C4	I2C.SR.SDA	D	I/O	IO.1P8	IO.1P8	2.5		3.4				12
B5	VMODE2	D	I	IO.1P8	IO.1P8							2
	I2C.SR.SCL	D	I/O	IO.1P8	IO.1P8	2.5		3.4				12
E5	I2C.CNTL.SDA	D	I/O	IO.1P8	IO.1P8	2.5		3.4				12
D5	I2C.CNTL.SCL	D	I	IO.1P8	IO.1P8	2.5		3.4				12
M1	PCM.VCK	D	I/O	IO.1P8	IO.1P8							2
L4	PCM.VDR	D	I/O	IO.1P8	IO.1P8							2
H8	PCM.VDX	D	I/O	IO.1P8	IO.1P8							2
N12	PCM.VFS	D	I/O	IO.1P8	IO.1P8							2
J4	I2S.CLK	D	I/O	IO.1P8	IO.1P8							2
K2	I2S.SYNC	D	I/O	IO.1P8	IO.1P8							2
H3	I2S.DIN	D	I	IO.1P8	IO.1P8							2
H4	I2S.DOUT	D	O	IO.1P8	IO.1P8							2
D2	MIC.MAIN.P	A	I	VINTANA1.OUT	MICBIAS1.OUT							
E2	MIC.MAIN.M	A	I	VINTANA1.OUT	MICBIAS1.OUT							
F5	MIC.SUB.P	A	I	VINTANA1.OUT	MICBIAS2.OUT							
	DIG.MIC.0	A	I	VINTANA1.OUT	VMIC1.OUT							
G5	MIC.SUB.M	A	I	VINTANA1.OUT	MICBIAS2.OUT							
E4	HSMIC.P	A	I	VINTANA1.OUT	VINTANA2.OUT							
E3	HSMIC.M	A	I	VINTANA1.OUT	VINTANA2.OUT							
A7	VBAT.LEFT	A	Power	VINTANA1.OUT[2]	VBAT							
B8	IHF.LEFT.P	A	O	VINTANA1.OUT[2]	VBAT							
A8	IHF.LEFT.M	A	O	VINTANA1.OUT[2]	VBAT							
C8	GND.LEFT	A	Power GND	None	GND							
A10	VBAT.RIGHT	A	Power	VINTANA1.OUT[2]	VBAT							
B9	IHF.RIGHT.P	A	O	VINTANA1.OUT[2]	VBAT							
A9	IHF.RIGHT.M	A	O	VINTANA1.OUT[2]	VBAT							
C9	GND.RIGHT	A	Power GND	None	GND							
C6	EAR.P	A	O	IO.1P8[2]	VINTANA2.OUT							
D6	EAR.M	A	O	IO.1P8[2]	VINTANA2.OUT							
C5	HSOL	A	O	IO.1P8[2]	VINTANA2.OUT							

Table 2-1. Ball Characteristics (continued)

BALL [1]	PIN NAME[2]	A/D [3]	TYPE [4]	ESD RAIL[8][3] VDD	REFERENCE LEVEL RL[5]	PU[6] (kΩ)[4]			PD[6] (kΩ)[4]			BUFFER STRENGTH (mA)[7]
						MIN	TYP	MAX	MIN	TYP	MAX	
E6	PreDriv.LEFT	A	O	IO.1P8[2]	VINTANA2.OUT							
	VMID	A	Power	IO.1P8[2]	VINTANA2.OUT							
A5	HSOR	A	O	IO.1P8[2]	VINTANA2.OUT							
D7	PreDriv.RIGHT	A	O	IO.1P8[2]	VINTANA2.OUT							
	ADCIN7	A	I	IO.1P8[2]	VINTANA2.OUT							
E1	AUXL	A	I	VINTANA1.OUT	VINTANA2.OUT							
F3	AUXR	A	I	VINTANA1.OUT	VINTANA2.OUT							
B1	MICBIAS1.OUT	A	Power	VINTANA2.OUT	VINTANA2.OUT							
	VMIC1.OUT	A	Power	VINTANA2.OUT	VINTANA2.OUT							
C1	MICBIAS2.OUT	A	Power	VINTANA2.OUT	VINTANA2.OUT							
	VMIC2.OUT	A	Power	VINTANA2.OUT	VINTANA2.OUT							
D3	VHSMIC.OUT	A	Power	VINTANA2.OUT	VINTANA2.OUT							
D1	MICBIAS.GND		Power GND	None	GND							
G4	AVSS1	A	Power GND	None	GND							
K7	AVSS2	A	Power GND	None	GND							
K11	AVSS3	A	Power GND	None	GND							
A6	AVSS4	A	Power GND	None	GND							
K8	ADCIN3	A	I	VUSB.3P1	VINTANA2.OUT							
K9	MANU_BRIX	D	O	IO.1P8	IO.1P8							
J6	32KCLKOUT	D	O	IO.1P8	IO.1P8							
L12	32KXIN	A	I	VRTC.OUT	IO.1P8							
L13	32KXOUT	A	O	VRTC.OUT	IO.1P8							
B11	HFCLKIN	A	I	IO.1P8	IO.1P8							
N8	HFCLKOUT	D	O	IO.1P8	IO.1P8							
H7	VBUS	A	Power	None	VBUS							
J7	DP/UART3.RXD	A	I/O	None	VBUS							2
J8	DN/UART3.TXD	A	I/O	None	VBUS							2
L8	ID	A	I/O	None	VBUS							2
J9	UCLK	D	I/O	IO.1P8	IO.1P8							16
K10	STP	D	I	IO.1P8	IO.1P8	75	100	202	59	100	144	16
	GPIO.9	D	I/O	IO.1P8	IO.1P8							2
J10	DIR	D	O	IO.1P8	IO.1P8	75	100	202	59	100	144	16
	GPIO.10	D	I/O	IO.1P8	IO.1P8							2
J11	NXT	D	O	IO.1P8	IO.1P8	75	100	202	59	100	144	16
	GPIO.11	D	I/O	IO.1P8	IO.1P8							2
H11	DATA0	D	I/O	IO.1P8	IO.1P8							16
	UART4.TXD	D	I	IO.1P8	IO.1P8							
H10	DATA1	D	I/O	IO.1P8	IO.1P8							16
	UART4.RXD	D	O	IO.1P8	IO.1P8							2
G8	DATA2	D	I/O	IO.1P8	IO.1P8							16
H9	DATA3	D	I/O	IO.1P8	IO.1P8	60	100	140	60	100	140	16
	GPIO.12	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	16

Table 2-1. Ball Characteristics (continued)

BALL [1]	PIN NAME[2]	A/D [3]	TYPE [4]	ESD RAIL[8](3) VDD	REFERENCE LEVEL RL[5]	PU[6] (kΩ)(4)			PD[6] (kΩ)(4)			BUFFER STRENGTH (mA)[7]
						MIN	TYP	MAX	MIN	TYP	MAX	
F9	DATA4	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	16
	GPIO.14	D	I/O	IO.1P8	IO.1P8							2
F8	DATA5	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	16
	GPIO.3	D	I/O	IO.1P8	IO.1P8							2
E10	DATA6	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	16
	GPIO.4	D	I/O	IO.1P8	IO.1P8							2
E11	DATA7	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	16
	GPIO.5	D	I/O	IO.1P8	IO.1P8							2
N13	TEST.RESET	A/D	I	None	VBAT				30	50	70	
N1	TESTV1	A	I/O	None	VBAT							
A13	TESTV2	A	I/O	IO.1P8(2)	VINTANA2.OUT							
A1	TEST	D	I	IO.1P8	IO.1P8				60	100	146	
B12	JTAG.TDI/ BERDATA	D	I	IO.1P8	IO.1P8							
D11	JTAG.TCK/ BERCLK	D	I	IO.1P8	IO.1P8							
M5	CP.IN	A	Power	None	VBAT/VBUS							
N6	CP.CAPP	A	O	VINTUSB1P8.OUT(2)	CP.CAPP							
N5	CP.CAPM	A	O	VINTUSB1P8.OUT(2)	CP.CAPM							
K5	CP.GND	A	Power GND	None	GND							
L6	VUSBIN.CPOUT	A	Power	None	VBAT							
N7	VBAT.USB	A	Power	None	VBAT							
L7	VUSB.3P1	A	Power	VUSB.3P1	VUSB.3P1							
H1	VAUX12S.IN	A	Power	None	VBAT							
J2	VAUX1.OUT	A	Power	VAUX1.OUT	VAUX1.OUT							
J1	VAUX2.OUT	A	Power	VAUX2.OUT	VAUX2.OUT							
F13	VPLLA3R.IN	A	Power	AGND	VBAT							
G12	VRTC.OUT	A	Power	None	VRTC.OUT							
G9	VPLL1.OUT	A	Power	VPPL1.OUT	VPLL1.OUT							
G13	VPLL2.OUT	A	Power	VPLL2.OUT	VPLL2.OUT							
F12	VAUX3.OUT	A	Power	VAUX3.OUT	VAUX3.OUT							
A2	VAUX4.IN	A	Power	None	VBAT							
B3	VAUX4.OUT	A	Power	VAUX4.OUT	VAUX4.OUT							
C2	VMMC1.IN	A	Power	None	VBAT							
B2	VMMC1.OUT	A	Power	VMMC1.OUT	VMMC1.OUT							
A4	VMMC2.IN	A	Power	None	VBAT							
B4	VMMC2.OUT	A	Power	VMMC2.OUT	VMMC2.OUT							
G2	VSL.OUT	A	Power	IO.1P8(2)	VSL.OUT							
M6	VINTUSB1P5.OUT	A	Power	None	VINTUSB1P5.OUT							
M7	VINTUSB1P8.OUT	A	Power	None	VINTUSB1P8.OUT							
G1	VDAC.IN	A	Power	None	VBAT							
H2	VDAC.OUT	A	Power	VDAC.OUT	VDAC.OUT							
H13	VINT.IN	A	Power	None	VBAT							

Table 2-1. Ball Characteristics (continued)

BALL [1]	PIN NAME[2]	A/D [3]	TYPE [4]	ESD RAIL[8](3) VDD	REFERENCE LEVEL RL[5]	PU[6] (kΩ)(4)			PD[6] (kΩ)(4)			BUFFER STRENGTH (mA)[7]
						MIN	TYP	MAX	MIN	TYP	MAX	
F2	VINTANA1.OUT	A	Power	None	VINTANA1.OUT							
B6	VINTANA2.OUT	A	Power	VINTANA2.OUT	VINTANA2.OUT							
F1	VINTANA2.OUT	A	Power	VINTANA2.OUT	VINTANA2.OUT							
H12	VINTDIG.OUT	A	Power	None	VINTDIG.OUT							
E12	VDD1.IN	A	Power	VINTDIG.OUT(2)	VBAT							
E13	VDD1.IN	A	Power	VINTDIG.OUT(2)	VBAT							
D12	VDD1.SW	A	O	VDD1.IN	VBAT							
D13	VDD1.SW	A	O	VDD1.IN	VBAT							
D10	VDD1.FB	A	I	None								
C12	VDD1.GND	A	Power GND	None	GND							
C13	VDD1.GND	A	Power GND	None	GND							
N9	VDD2.IN	A	Power	VINTDIG.OUT(2)	VBAT							
M9	VDD2.IN	A	Power	VINTDIG.OUT(2)	VBAT							
M12	VDD2.FB	A	I	None								
M10	VDD2.SW	A	O	VDD2.IN	VBAT							
N10	VDD2.SW	A	O	VDD2.IN	VBAT							
M11	VDD2.GND	A	Power GND	None	GND							
N11	VDD2.GND	A	Power GND	None	GND							
M4	VIO.IN	A	Power	VINTDIG.OUT(2)	VBAT							
N4	VIO.IN	A	Power	VINTDIG.OUT(2)	VBAT							
L2	VIO.FB	A	I	None								
M3	VIO.SW	A	O	VIO.IN	VBAT							
N3	VIO.SW	A	O	VIO.IN	VBAT							
N2	VIO.GND	A	Power GND	None	GND							
M2	VIO.GND	A	Power GND	None	GND							
L3	VIO.GND	A	Power GND	None	GND							
J12	BKBAT	A	Power	BKBAT	VBACK							
E7	IO.1P8	A	Power	None	IO.1P8							
G11	DGND	A	Power GND	None	GND							
F10	LEDGND	A	Power GND	None	GND							
A12	GPIO.13	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	
	LEDSYNC	D	I	IO.1P8	IO.1P8							
E9	LEDA	A	Open Drain	IO.1P8(2)	VBAT							
	VIBRA.P	A	Open Drain	IO.1P8(2)	VBAT							
F11	LEDB	A	Open Drain	IO.1P8(2)	VBAT							
	VIBRA.M	A	Open Drain	IO.1P8(2)	VBAT							
D9	VBATVIBRA	A	Power	IO.1P8(2)	VBAT							

Table 2-1. Ball Characteristics (continued)

BALL [1]	PIN NAME[2]	A/D [3]	TYPE [4]	ESD RAIL[8](3) VDD	REFERENCE LEVEL RL[5]	PU[6] (kΩ)(4)			PD[6] (kΩ)(4)			BUFFER STRENGTH (mA)[7]
						MIN	TYP	MAX	MIN	TYP	MAX	
C3	GPIO.16	D	I/O	IO.1P8	IO.1P8	75	100	202	59	100	144	
	DIG.MIC.CLK0	D	O	IO.1P8	IO.1P8							

(1) To avoid reflection on this pin due to impedance mismatch, a serial resistance of 33 Ω needs to be added.

(2) VDD rail used as bias in ESD protection during functional mode.

(3) AGND is used as ESD Ground for all PADs.

(4) PUs/PDs are enabled when TPS65952 is in any other state than NO SUPPLY

2.2.1 *ESD Electrical Parameters*

ESD conditions for CDM and HBM listed in Table 2-2.

Table 2-2. ESD Electrical Parameters

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CDM stress voltage	All pads	500			V
HBM stress voltage	All pads	2000			V

2.3 Ball Placement (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	TEST	VAUX4.IN	Reserved	VMMC2.IN	HSOR	AVSS4	VBAT.LEFT	IHF.LEFT.M	IHF.RIGHT.M	VBAT.RIGHT	NRESWARM	LEDSYNC/ GPIO.13	TESTV2	A
B	MICBIAS1. OUT/ VMIC1.OUT	VMMC1.OUT	VAUX4.OUT	VMMC2.OUT	VMODE2/ I2C.SR.SCL	VINTANA2 .OUT	MSECURE	IHF.LEFT.P	IHF.RIGHT.P	INT1	HFCLKIN	JTAG.TDI/ BERDATA	CLKREQ	B
C	MICBIAS2. OUT/ VMIC2.OUT	VMMC1.IN	GPIO16/ DIG.MIC. CLK0	I2C.SR.SDA	HSOL	EAR.P	Reserved	GND.LEFT	GND.RIGHT	NRESPWRON	NSLEEP1	VDD1.GND	VDD1.GND	C
D	MICBIAS. GND	MIC.MAIN.P	VHSMIC.OUT	Reserved	I2C.CNTL. SCL	EAR.M	PreDriv. RIGHT/ ADCIN7	REGEN	VBATVIBRA	VDD1.FB	JTAG.TCK/ BERCLK	VDD1.SW	VDD1.SW	D
E	AUXL	MIC.MAIN.M	HSMIC.M	HSMIC.P	I2C.CNTL. SDA	PreDriv .LEFT/ VMID	IO.1P8	SYSEN	LEDA/ VIBRA.P	DATA6/ GPIO.4	DATA7/ GPIO.5	VDD1.IN	VDD1.IN	E
F	VINTANA2. OUT	VINTANA1. OUT	AUXR	ADCIN2	MIC.SUB./ DIG.MIC.0	CLKEN	PWRON	DATA5/ GPIO.3	DATA4/ GPIO.14	LEDGND	LEDB/ VIBRA.M	VAUX3.OUT	VPLLA3R.IN	F
G	VDAC.IN	VSL.OUT	ADCIN1	AVSS1	MIC.SUB.M	Reserved	AGND	DATA2	VPPL1.OUT	BOOT1	DGND	VRTC.OUT	VPLL2.OUT	G
H	VAUX12S.IN	VDAC.OUT	I2S.DIN	I2S.DOUT	USBCHRG _STATZ	Reserved	VBUS	PCM.VDX	DATA3/ GPIO.12	DATA1/ UART4.RXD	DATA0/ UART4.TXD	VINTDIG.OUT	VINT.IN	H
J	VAUX2.OUT	VAUX1.OUT	GPIO.2/ TEST1	I2S.CLK	USBCHRG _ENZ	32KCLKOUT	DP/UART3. RXD	DN/ UART3.TXD	UCLK	DIR/ GPIO.10	NXT/ GPIO.11	BKBAT	BOOT0	J
K	ADCIN0	I2S.SYNC	GPIO6/ CLKOK/ PWM0/ TEST3	VPROG	CP.GND	CHRG_ DET_N	AVSS2	ADCIN3	MANU_BRIX	STP/GPIO.9	AVSS3	VREFGND	VREF	K
L	VPRECH	VIO.FB	VIO.GND	PCM.VDR	VBAT	VUSBIN. CPOUT	VUSB.3P1	ID	GPIO.1/CD2/ JTAG.TMS	GPIO.15/ TEST2	START.ADC	32KXIN	32KXOUT	L
M	PCM.VCK	VIO.GND	VIO.SW	VIO.IN	CP.IN	VINTUSB1 P5.OUT	VINTUSB1 P8.OUT	GPIO.0/CD1/ JTAG.TD0	VDD2.IN	VDD2.SW	VDD2.GND	VDD2.FB	GPIO.7/ VIBRA.SY NC.PWM1/ TEST4	M
N	TESTV1	VIO.GND	VIO.SW	VIO.IN	CP.CAPM	CP.CAPP	VBAT.USB	HFCLKOUT	VDD2.IN	VDD2.SW	VDD2.GND	PCM.VFS	TEST.RES ET	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

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Figure 2-2. Top View

2.4 Signal Description

Table 2-3 provides a description of the signals on the TPS65951; some signals are available on multiple pins.

Table 2-3. Signal Description

MODULE	SIGNAL NAME	DESCRIPTION	TYPE	BALLS	CONFIGURATION BY DEFAULT AFTER RESET RELEASED			NOT USED FEATURES(1)
					SIGNAL	TYPE	INTERNAL PULL OR NOT	
ADC	ADCIN0	Battery type	I/O	K1	ADCIN0	I		Floating
	ADCIN1	Battery temperature	I/O	G3	ADCIN1	I		Floating
	ADCIN2	General-purpose ADC input	I	F4	ADCIN2	I		Floating
	ADCIN3	General-purpose ADC input 3	I	K8	ADCIN3	I		Floating
Charger	VPROG	EEPROM programming voltage	I	K4	VPROG	I		GND
	VPRECH	Precharge regulator output	O	L1	VPRECH	O		Cap to GND(3)
	VBAT	Battery voltage sensing	Power	L5	VBAT	Power		VBAT
	CHRG_DET_N	USB Charger Detection (100 mA/500 mA)	O	K6	CHRG_DET_N	O		Floating
	USBCHRG_ENZ	USB charger enable Z	O	J5	USBCHRG_ENZ	O		Floating
	USBCHRG_STATZ	USB charger status	I	H5	USBCHRG_STATZ	I	PU	Floating
	MANU_BRIX	Battery Removal Indicator	O	K9	MANU_BRIX	O		Floating
GPIOs / JTAG	GPIO.0/CD1	GPIO0/card detection 1	I/O	M8	GPIO.0	I	PD	Floating
	JTAG.TDO	JTAG test data output	I/O					
	GPIO.1/CD2	GPIO1/card detection 2	I/O	L9	GPIO.1	I	PD	Floating
	JTAG.TMS	JTAG test mode state	I					
	GPIO.2	GPIO2	I/O	J3	GPIO.2	I	PD	Floating
	TEST1	TEST1 pin used in test mode only	I/O					
	GPIO.15	GPIO15	I/O	L10	GPIO.15	I	PD	Floating
	TEST2	TEST2 pin used in test mode only	I/O					
	GPIO.6	GPIO6	I/O	K3	GPIO.6	I	PD	Floating
	PWM0	Pulse width driver 0	O					
	TEST3	TEST3 pin used in test mode only (controlled by JTAG)	I/O					
	CLKOK							
	GPIO.7	GPIO.7	I/O	M13	GPIO.7	I	PD	Floating
	VIBRA.SYNC	Vibrator on-off synchronization	I					
	PWM1	Pulse width driver	O					
	TEST4	TEST4 pin used in test mode only (controlled by JTAG)	I/O					
START. ADC	START.ADC	ADC conversion request	I	L11	START.ADC	I		GND

Table 2-3. Signal Description (continued)

MODULE	SIGNAL NAME	DESCRIPTION	TYPE	BALLS	CONFIGURATION BY DEFAULT AFTER RESET RELEASED			NOT USED FEATURES[1]
					SIGNAL	TYPE	INTERNAL PULL OR NOT	
CONTROL	SYSEN	System enable output	Open drain/I	E8	SYSEN	OD	PU	Floating
	CLKEN	Clock enable	O	F6	CLKEN	O		Floating
	CLKREQ	Clock request	I	B13	CLKREQ	I	PD	GND
	INT1	Output interrupt line 1	O	B10	INT1	O		Floating
	NRESPWRON	Output control the NRESPWRON of the application processor	O	C10	NRESPWRON	O		Floating
	NRESWARM	Input, detect user action on the reset button	I	A11	NRESWARM	I		GND
	PWRON	Input, detect a control command to start or stop the system	I	F7	PWRON	I		VBAT
	NSLEEP1	Sleep request from device 1	I	C11	NSLEEP1	I		GND
	BOOT0	Boot pin 0	I	J13	BOOT0	I	PD	Not Applicable
	BOOT1	Boot pin 1	I	G10	BOOT1	I	PD	Not Applicable
	REGEN	Enable signal for external LDO	Open Drain	D8	REGEN	OD	PU	Floating
	MSECURE	Security and digital rights management	I	B7	MSECURE	I		IO.1P8
VREF	VREFGND	Reference voltage ground	Power GND	K12	VREFGND	Power GND		GND
	VREF	Reference voltage	Power	K13	VREF	Power		Not Applicable
	AGND	Analog ground for reference voltage	Power GND	G7	AGND	Power GND		GND
I^{2}C SmartReflex	I2C.SR.SDA	SmartReflex I^{2}C data	I/O	C4	Signal not functional[2]			Floating
	VMODE2	Digital voltage scaling linked with VDD2	I	B5	VMODE2	I		GND
	I2C.SR.SCL	SmartReflex I^{2}C data	I/O					
I^{2}C	I2C.CNTL.SDA	General-purpose I^{2}C data	I/O	E5	I2C.CNTL.SDA	IO	PU	Not Applicable
	I2C.CNTL.SCL	General-purpose I^{2}C clock	I/O	D5	I2C.CNTL.SCL	IO	PU	Not Applicable
PCM	PCM.VCK	Data clock (voice port)	I/O	M1	PCM.VCK	IO		Floating
	PCM.VDR	Data receive (voice port)	I/O	L4	PCM.VDR	IO		GND
	PCM.VDX	Data transmit (voice port)	I/O	H8	PCM.VDX	IO		Floating
	PCM.VFS	Frame synchronization (voice port)	I/O	N12	PCM.VFS	IO		Floating
TDM	I2S.CLK	Clock signal (audio port)	I/O	J4	I2S.CLK	IO		Floating
	I2S.SYNC	Synchronization signal (audio port)	I/O	K2	I2S.SYNC	IO		Floating
	I2S.DIN	Data receive (audio port)	I	H3	I2S.DIN	I		GND
	I2S.DOUT	Data transmit (audio port)	O	H4	I2S.DOUT	O		Floating

Table 2-3. Signal Description (continued)

MODULE	SIGNAL NAME	DESCRIPTION	TYPE	BALLS	CONFIGURATION BY DEFAULT AFTER RESET RELEASED			NOT USED FEATURES[(1)]
					SIGNAL	TYPE	INTERNAL PULL OR NOT	
ANA.MIC	MIC.MAIN.P	Main microphone left input (P)	I	D2	MIC.MAIN.P	I		Cap to GND
	MIC.MAIN.M	Main microphone left input (M)	I	E2	MIC.MAIN.M	I		Cap to GND
	MIC.SUB.P	Main microphone right input (P)	I	F5	MIC.SUB.P	I		Cap to GND
	DIG.MIC.0	Digital microphone 0 input data	I					
	MIC.SUB.M	Main microphone right input (M)	I	G5	MIC.SUB.M	I		Cap to GND
Headset Microphone	HSMIC.P	Headset microphone input (P)	I	E4	HSMIC.P	I		Cap to GND
	HSMIC.M	Headset microphone input (M)	I	E3	HSMIC.M	I		Cap to GND
Hands-Free	VBAT.LEFT	Battery voltage input	Power	A7	VBAT.LEFT	Power		VBAT
	IHF.LEFT.P	Hands-free speaker output left (P)	O	B8	IHF.LEFT.P	O		Floating
	IHF.LEFT.M	Hands-free speaker output left (M)	O	A8	IHF.LEFT.M	O		Floating
	GND.LEFT	GND	Power GND	C8	GND.LEFT	Power GND		GND
	VBAT.RIGHT	Battery voltage input	Power	A10	VBAT.RIGHT	Power		VBAT
	GND.RIGHT	GND	Power GND	C9	GND.RIGHT	Power GND		GND
	IHF.RIGHT.P	Hands-free speaker output right (P)	O	B9	IHF.RIGHT.P	O		Floating
	IHF.RIGHT.M	Hands-free speaker output right (M)	O	A9	IHF.RIGHT.M	O		Floating
Earpiece	EAR.P	Earpiece output differential output (P)	O	C6	EAR.P	O		Floating
	EAR.M	Earpiece output differential output (M)	O	D6	EAR.M	O		Floating
Headset	HSOL	Differential/single-ended headset left output	O	C5	HSOL	O		Floating
	PreDriv.LEFT	Predriver output left P for external class D amplifier	O	E6	VMID	Power		Floating
	VMID		Power					
	HSOR	Differential/single-ended headset right output (P)	O	A5	HSOR	O		Floating
	PreDriv.RIGHT	Predriver output right P for external class D amplifier	O	D7	ADCIN7	I		GND
	ADCIN7	General-purpose ADC input 7	I					
AUX Input	AUXL	Auxiliary audio input left	I	E1	AUXL	I		Cap to GND
	AUXR	Auxiliary audio input right	I	F3	AUXR	I		Cap to GND

Table 2-3. Signal Description (continued)

MODULE	SIGNAL NAME	DESCRIPTION	TYPE	BALLS	CONFIGURATION BY DEFAULT AFTER RESET RELEASED			NOT USED FEATURES(1)
					SIGNAL	TYPE	INTERNAL PULL OR NOT	
VMIC Bias	MICBIAS1.OUT	Analog microphone bias 1	Power	B1	MICBIAS1.OUT	Power		Floating
	VMIC1.OUT	Digital microphone power supply 1	Power					
	MICBIAS2.OUT	Analog microphone bias 2	Power	C1	MICBIAS2.OUT	Power		Floating
	VMIC2.OUT	Digital microphone power supply 2	Power					
	VHSMIC.OUT	Headset microphone bias	Power	D3	VHSMIC.OUT	Power		Floating
	MICBIAS.GND	Dedicated ground for microphones	Power GND	D1	MICBIAS.GND	Power GND		GND
	AVSS1	Analog ground	Power GND	G4	AVSS1	Power GND		GND
	AVSS2			K7	AVSS2			
	AVSS3			K11	AVSS3			
	AVSS4			A6	AVSS4			
CLOCK	32KCLKOUT	Buffered output of the 32-kHz digital clock	O	J6	32KCLKOUT	O		Floating
	32KXIN	Input of the 32-kHz oscillator	I	L12	32KXIN	I		Not Applicable
	32KXOUT	Output of the 32-kHz oscillator	O	L13	32KXOUT	O		Floating
	HFCLKIN	Input of the digital (or sine) high-speed clock	I	B11	HFCLKIN	I		Not Applicable
	HFCLKOUT	High-speed clock output	O	N8	HFCLKOUT	O		Floating
USB PHY	VBUS	VBUS power rail	Power	H7	VBUS	Power		Not Applicable
	DP/ UART3.RXD	USB data P/USB car-kit receive data/UART3 receive data	I/O	J7	DP/UART3.RXD	IO		Not Applicable
	DN/ UART3.TXD	USB data N/USB car-kit transmit data/UART3 transmit data	I/O	J8	DN/UART3.TXD	IO		Not Applicable
	ID	USB ID	I/O	L8	ID	IO		Floating

Table 2-3. Signal Description (continued)

MODULE	SIGNAL NAME	DESCRIPTION	TYPE	BALLS	CONFIGURATION BY DEFAULT AFTER RESET RELEASED			NOT USED FEATURES[(1)]
					SIGNAL	TYPE	INTERNAL PULL OR NOT	
ULPI	UCLK	High-speed USB clock	I/O	J9	UCLK	O		Floating
	STP	High-speed USB stop	I	K10	STP	I	PU	Floating
	GPIO.9	GPIO.9	I/O					
	DIR	High-speed USB direction	O	J10	DIR	O		Floating
	GPIO.10	GPIO.10	I/O					
	NXT	High-speed USB next	O	J11	NXT	O		Floating
	GPIO.11	GPIO.11	I/O					
	DATA0	High-speed USB Data0	I/O	H11	DATA0	O		Floating
	UART4.TXD	UART4.TXD	I					
	DATA1	High-speed USB Data1	I/O	H10	DATA1	O		Floating
	UART4.RXD	UART4.RXD	O					
	DATA2	High-speed USB Data2	I/O	G8	DATA2	O		Floating
	DATA3	High-speed USB Data3	I/O	H9	DATA3	O		Floating
	GPIO.12	GPIO.12	I/O					
	DATA4	High-speed USB Data4	I/O	F9	DATA4	O		Floating
	GPIO.14	GPIO.14	I/O					
	DATA5	High-speed USB Data5	I/O	F8	DATA5	O		Floating
	GPIO.3	GPIO.3	I/O					
	DATA6	High-speed USB Data6	I/O	E10	DATA6	O		Floating
	GPIO.4	GPIO.4	I/O					
	DATA7	High-speed USB Data7	I/O	E11	DATA7	O		Floating
	GPIO.5	GPIO.5	I/O					
TEST	TEST.RESET	Reset T2 device (except power state-machine)	I	N13	TEST.RESET	I	PD	GND
	TESTV1	Analog test	I/O	N1	TESTV1	IO		Floating
	TESTV2	Analog test	I/O	A13	TESTV2	IO		Floating
	TEST	Selection between JTAG mode and application mode for JTAG/GPIOs (with PU or PD)	I	A1	TEST	I	PD	Floating
	JTAG.TDI/ BERDATA	JTAG.TDI/BERDATA	I	B12	JTAG.TDI/ BERDATA	I		GND
	JTAG.TCK/ BERCLK	JTAG.TCK/BERCLK	I	D11	JTAG.TCK/ BERCLK	I		GND
USB CP	CP.IN	Charge pump input voltage	Power	M5	CP.IN	Power		VBAT
	CP.CAPP	Charge pump flying capacitor P	O	N6	CP.CAPP	O		Floating
	CP.CAPM	Charge pump flying capacitor M	O	N5	CP.CAPM	O		Floating
	VUSBIN.CPOUT	Char pump output USBLDO3P3 input		L6		Power		
	CP.GND	Charge pump ground	Power GND	K5	CP.GND	Power GND		GND
VBAT.USB	VBAT.USB	USB LDOs (VINTUSB1P5, VINTUSB1P8, VUSB.3P1) VBAT	Power	N7	VBAT.USB	Power		VBAT

Table 2-3. Signal Description (continued)

MODULE	SIGNAL NAME	DESCRIPTION	TYPE	BALLS	CONFIGURATION BY DEFAULT AFTER RESET RELEASED			NOT USED FEATURES(1)
					SIGNAL	TYPE	INTERNAL PULL OR NOT	
USB.LDO	VUSB.3P1	USB LDO output	Power	L7	VUSB.3P1	Power		Not Applicable
VAUX1	VAUX12S.IN	VAUX1/VAUX2 LDO input voltage	Power	H1	VAUX12S.IN	Power		VBAT
	VAUX1.OUT	VAUX1 LDO output voltage	Power	J2	VAUX1.OUT	Power		Floating
VAUX2	VAUX2.OUT	VAUX2 LDO output voltage	Power	J1	VAUX2.OUT	Power		Floating
VPLLA3R	VPLLA3R.IN	Input for VPLL1, VPLL2, VAUX3, VRTC LDOs	Power	F13	VPLLA3R.IN	Power		VBAT
VRTC	VRTC.OUT	VRTC internal LDO output (internal use only)	Power	G12	VRTC.OUT	Power		Not Applicable
VPLL1	VPLL1.OUT	LDO output voltage	Power	G9	VPLL1.OUT	Power		Floating
VPLL2	VPLL2.OUT	Output voltage of the regulator	Power	G13	VPLL2.OUT	Power		Floating
VAUX3	VAUX3.OUT	VAUX3 LDO output voltage	Power	F12	VAUX3.OUT	Power		Floating
VAUX4	VAUX4.IN	VAUX4 LDO input voltage	Power	A2	VAUX4.IN	Power		VBAT
	VAUX4.OUT	VAUX4 LDO output voltage	Power	B3	VAUX4.OUT	Power		Floating
VMMC1	VMMC1.IN	VMMC1 LDO input voltage	Power	C2	VMMC1.IN	Power		VBAT
	VMMC1.OUT	VMMC1 LDO output voltage	Power	B2	VMMC1.OUT	Power		Floating
VMMC2	VMMC2.IN	VMMC2 LDO input voltage	Power	A4	VMMC2.IN	Power		VBAT
	VMMC2.OUT	VMMC2 LDO output voltage	Power	B4	VMMC2.OUT	Power		Floating
VSL	VSL.OUT	CHARGING led output	Power	G2	VSL.OUT	Power		Floating
VINTUSB1 P5	VINTUSB1P5.OUT	VINTUSB1P5 internal LDO output (internal use only)	Power	M6	VINTUSB1P5. OUT	Power		Floating
VINTUSB1 P8	VINTUSB1P8.OUT	VINTUSB1P8 internal LDO output (internal use only)	Power	M7	VINTUSB1P8. OUT	Power		Floating
Video DAC	VDAC.IN	Input for VDAC, VINTANA1, and VINTANA2 LDOs	Power	G1	VDAC.IN	Power		VBAT
	VDAC.OUT	Output voltage of the regulator	Power	H2	VDAC.OUT	Power		Floating
VINT	VINT.IN	Input for VINTDIG LDO	Power	H13	VINT.IN	Power		VBAT
VINTANA1	VINTANA1.OUT	VINTANA1 internal LDO output (internal use only)	Power	F2	VINTANA1.OUT	Power		Not Applicable
VINTANA2	VINTANA2.OUT	VINTANA2 internal LDO output (internal use only)	Power	B6	VINTANA2.OUT	Power		Not Applicable
	VINTANA2.OUT	VINTANA2 internal LDO output (internal use only)	Power	F1	VINTANA2.OUT	Power		Not Applicable
VINTDIG	VINTDIG.OUT	VINTDIG internal LDO output (internal use only)	Power	H12	VINTDIG.OUT	Power		Not Applicable

Table 2-3. Signal Description (continued)

MODULE	SIGNAL NAME	DESCRIPTION	TYPE	BALLS	CONFIGURATION BY DEFAULT AFTER RESET RELEASED			NOT USED FEATURES[(1)]
					SIGNAL	TYPE	INTERNAL PULL OR NOT	
VDD1	VDD1.IN	VDD1 DC-DC input voltage	Power	E12	VDD1.IN	Power		VBAT
	VDD1.IN	VDD1 DC-DC input voltage	Power	E13	VDD1.IN	Power		VBAT
	VDD1.SW	VDD1 DC-DC switch	O	D12	VDD1.SW	O		Floating
	VDD1.SW	VDD1 DC-DC switch	O	D13	VDD1.SW	O		Floating
	VDD1.FB	VDD1 DC-DC output voltage (feedback)	I	D10	VDD1.FB	I		GND
	VDD1.GND	VDD1 DC-DC ground	Power GND	C12	VDD1.GND	Power GND		GND
	VDD1.GND	VDD1 DC-DC ground	Power GND	C13	VDD1.GND	Power GND		GND
VDD2	VDD2.IN	VDD2 DC-DC input voltage	Power	N9	VDD2.IN	Power		VBAT
	VDD2.IN	VDD2 DC-DC input voltage	Power	M9	VDD2.IN	Power		VBAT
	VDD2.FB	VDD2 DC-DC output voltage (feedback)	I	M12	VDD2.FB	I		GND
	VDD2.SW	VDD2 DC-DC switch	O	M10	VDD2.SW	O		Floating
	VDD2.SW	VDD2 DC-DC switch	O	N10	VDD2.SW	O		Floating
	VDD2.GND	VDD2 DC-DC ground	Power GND	M11	VDD2.GND	Power GND		GND
	VDD2.GND	VDD2 DC-DC ground	Power GND	N11	VDD2.GND	Power GND		GND
VIO	VIO.IN	VIO DC-DC input voltage	Power	M4	VIO.IN	Power		VBAT[(4)]
	VIO.IN	VIO DC-DC input voltage	Power	N4	VIO.IN	Power		VBAT[(4)]
	VIO.FB	VIO DC-DC output voltage (feedback)	I	L2	VIO.FB	I		GND
	VIO.SW	VIO DC-DC switch	O	M3	VIO.SW	O		Floating
	VIO.SW	VIO DC-DC switch	O	N3	VIO.SW	O		Floating
	VIO.GND	VIO DC-DC ground	Power GND	N2	VIO.GND	Power GND		GND
	VIO.GND	VIO DC-DC ground	Power GND	L3	VIO.GND	Power GND		GND
	VIO.GND	VIO DC-DC ground	Power GND	M2	VIO.GND	Power GND		GND
Backup Bat	BKBAT	Backup battery	Power	J12	BKBAT	Power		GND
Digital VDD	IO.1P8	TPS65951 IO input	Power	E7	IO.1P8	Power		Not Applicable
Digital ground	DGND	Digital ground	Power GND	G11	DGND	Power GND		GND

Table 2-3. Signal Description (continued)

MODULE	SIGNAL NAME	DESCRIPTION	TYPE	BALLS	CONFIGURATION BY DEFAULT AFTER RESET RELEASED			NOT USED FEATURES(1)
					SIGNAL	TYPE	INTERNAL PULL OR NOT	
LED driver	VBAT.VIBRA	H-Bridge Vibra VBAT	Power	D9	VBAT.VIBRA	Power		VBAT
	LEDGND	LED driver ground	Power GND	F10	LEDGND	Power GND		GND
	GPIO.13	GPIO.13	I/O	A12	GPIO.13	I	PD	Floating
	LEDSYNC	LED synchronization input	I					
	LEDA	LED leg A	Open Drain	E9	Signal not Functional(2)			Floating
	VIBRA.P	H-Bridge Vibra P						
	LEDB	LED leg B	Open Drain	F11	Signal not Functional(2)			Floating
	VIBRA.M	H-Bridge Vibra M						
Digital Microphone	GPIO.16	GPIO.16	I/O	C3	GPIO.16	I	PD	Floating
	DIG.MIC.CLK0	Digital microphone clock 0	O					

(1) This column provides the connection when the associated feature is not used or not connected. When there is pin multiplexing, we consider that all functions on the multiplexed pin are not used. But even if all functions are not used, we have to consider the configuration by default.

Special criteria: For audio features input, use capacitor to ground with a 100-nF typical value capacitor.
Not Applicable: When the associated feature is mandatory for the good working of TPS65951.

(2) Signal not functional indicates that no signal is present on the pad after a release reset.

(3) The signal VPRECH must be connected with the CPRECH capacitor to GND.

(4) VIO internal oscillator is used even if VIO output is not used; therefore, VIO has to be connected to VBAT.

2.5 Ground Connection Usage

Ground connections for different blocks are listed in Table 2-4.

Table 2-4. Ground Connections

CATEGORY	BLOCK	AVSS1	AVSS2	AVSS3	AVSS4	AGND	REFGND	DGND	VDD1.GND	VDD2.GND	VIO.GND	GND.LEFT	GND.RIGHT
Audio	Audio Uplink (TX)	X											
	Audio Downlink (RX)				X								
	Audio HF PLL	X											
	Hands-Free (class-D), Left											X	
	Hands-Free (class-D), Right												X
LDO	VDAC	X											
	VPLL1			X									
	VPLL2			X									
	VMMC1				X								
	VMMC2				X								
	VAUX1	X											
	VAUX2	X											
	VAUX3			X									
	VAUX4				X								
	VINTDIG			X									
	VINTANA1	X											
	VINTANA2	X											
	USB (including USB LDOs)		X										
	GPADC		X										
	BCI		X										
	EEPROM		X										
	BBS (Backup Battery System)			X									
	Clock Slicer			X									
DC-DC	VIO	X											
	VIO Dedicated Power Ground										X		
	VDD1			X									
	VDD1 Dedicated Power Ground								X				
	VDD2			X									
	VDD2 Dedicated Power Ground									X			
	Substrate Ground					X							
	Clean, extra low current, low noise ground used for all sensitive analog modules (including band-gap voltage, 32-kHz oscillator).						X						
	Digital audio filter and digital logic (all DGND balls are merged)							X					

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 lists the absolute maximum ratings.

Table 3-1. Absolute Maximum Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Main battery supply voltage (1)		0		5	V
Voltage on any input(2)	Where supply represents the voltage applied to the power supply pin associated with the input(3)	–0.3		1.0 × Supply + 0.3	V
VBUS inputs		-2		20	V
Storage temperature range		–55		125	°C
Ambient temperature range		–40		85	°C
Junction temperature (T_J)	Absolute maximum rating	–40		150	°C
Junction temperature (T_J)	For parametric compliance	–40		125	°C
Ambient temperature for parametric compliance	With max 125°C as Junction temperature (T_J)	–40		85	°C
DP, DM, ID high voltage short circuit	DP, DM, or ID pins short circuited to VBUS supply, in any mode of device operation, continuously for 24 hours			5.25	V
DP, DM, ID low voltage short circuit	DP, DM, or ID pins short circuited to GND in any mode of device operation, continuously for 24 hours	0			V

(1) The product will have negligible reliability impact if voltage spikes of 5.2 V occur for a total duration (cumulative over lifetime) of 10 milliseconds.

(2) Except VBAT input pads and VBUS pad.

(3) Supply equals the reference level listed in Table 2-1 for each pin.

3.2 Minimum Voltages and Associated Currents

Table 3-2. VBAT Min Required Per VBAT Ball and Associated Maximum Current

		Maximum Current Specified (mA)	Output Voltage (V)	VBAT min (V)
VBAT pin name	VPLLA3R.IN	340		
Internal module supplied	VPLL1 (LDO)	40	1.0 / 1.2 / 1.3 / 1.8	maximum (2.7, output voltage selected + 250 mV)
	VPLL2 (LDO)	100	0.7 / 1.0 / 1.2 / 1.3 / 1.8	maximum (2.7, output voltage selected + 250 mV)
	VAUX3 (LDO)	200	1.5 / 1.8 / 2.5 / 2.8	maximum (2.7, output voltage selected + 250 mV)
	VDD1 core (DCDC)	< 1		2.7
	VDD2 core (DCDC)	< 1		2.7
	SYSPOR (power ref)	< 1		2.7
	PBIAS (power ref)	< 1		2.7
VBAT pin name	VDAC.IN	370		

Table 3-2. VBAT Min Required Per VBAT Ball and Associated Maximum Current (continued)

		Maximum Current Specified (mA)	Output Voltage (V)	VBAT min (V)
Internal module supplied	VDAC (LDO)	70	1.2 / 1.3 / 1.8	maximum (2.7, output voltage selected + 250 mV)
	VINTANA1 (LDO)	50	1.5	maximum (2.7, output voltage selected + 250 mV)
	VINTANA2 (LDO)	250	2.5 / 2.75	maximum (2.7, output voltage selected + 250 mV)
	VIO core (DCDC)	< 1		2.7
	VAUX4 core (LDO)	< 1		2.7
VBAT pin name	VAUX12S.IN	350		
Internal module supplied	VAUX1 (LDO)	200	2.5 / 2.8 / 3.0	maximum (2.7, output voltage selected + 250 mV)
	VAUX2 (LDO)	100	1.3 / 1.5 / 1.7 / 1.8 / 1.9 / 2.0 / 2.1 / 2.2 / 2.3 / 2.4 / 2.5 / 2.8	maximum (2.7, output voltage selected + 250 mV)
VBAT pin name	VMMC2.IN	100		
	VMMC2 (LDO)	100	1.85 / 2.6 / 2.85 / 3.0 / 3.15	maximum (2.7, output voltage selected + 250 mV)
	POWER_REGBATT	0.001		2.7
VBAT pin name	VMMC1.IN	220		
	VMMC1 (LDO)	220	1.85 / 2.85 / 3.0 / 3.15	maximum (2.7, output voltage selected + 250 mV)
	POWER_REGBATT	0.001		2.7
VBAT pin name	VINTDIG.IN	131		
Internal module supplied	VINTDIG (LDO)	100	1.5	maximum (2.7, output voltage selected + 250 mV)
	VRRTC (LDO)	30	1.5	maximum (2.7, output voltage selected + 250 mV)
	VBRTC (LDO)	1	1.3	maximum (2.7, output voltage selected + 250 mV)
VBAT pin name	VAUX4.IN	100		
	VAUX4 (LDO)	100	0.7 / 1.0 / 1.2 / 1.3 / 1.5 / 1.8 / 2.5 / 2.8	output voltage selected + 250 mV

3.3 Recommended Operating Conditions

Table 3-3 lists the recommended operating maximum ratings.

Table 3-3. Recommended Operating Maximum Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Main battery supply voltage		2.7	3.6	4.5	V
Backup battery supply voltage		1.8	3.2	3.3	V
Ambient temperature range		–40		85	°C

3.4 Digital I/O Electrical Characteristics

Table 3-4 describes the digital I/O electrical characteristics.

- **RL:** Reference level voltage applied to the I/O cell
- **VOL:** Low-level output voltage
- **VOH:** High-level output voltage
- **VIL:** Low-level input voltage
- **VIH:** High-level input voltage

Table 3-4. Digital I/O Electrical Characteristics

Pin Name	VOL (V)		VOH (V)		VIL (V)		VIH (V)		MAX FREQ (MHz)	MAX LOAD (pF) OUTPUT MODE	MAX RISE[(1)] TIME (ns)	MAX FALL[(1)] TIME (ns)
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
GPIO.0/CD1 JTAG.TDO	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	33	30	5.2	5.2
GPIO.1/CD2 JTAG.TMS	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	33	30	5.2	5.2
GPIO.2 TEST1	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	3	30	5.2	5.2
GPIO.15 TEST2	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	3	30	5.2	5.2
GPIO.6 PWM0 TEST3	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	3	30	5.2	5.2
GPIO.7 VIBRA.SYNC PWM1 TEST4	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	3	30	5.2	5.2
START.ADC					0	0.35 × RL	0.65 × RL	RL	6		16.7	16.7
SYSEN	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL			5.2	5.2
CLKEN	0	0.45	RL – 0.45	RL					3	30	33.3	33.3
CLKREQ					0	0.35 × RL	0.65 × RL	RL	3		33.3	33.3
INT1	0	0.45	RL – 0.45	RL					3	30	33.3	33.3
NRESPWRON	0	0.45	RL – 0.45	RL					3	30	33.3	33.3
NRESWARM					0	0.35 × RL	0.65 × RL	RL	3	30	33.3	33.3
PWRON					0	0.35 × 1.8 V	0.65 × 1.8 V	VBAT	3		33.3	33.3
NSLEEP1					0	0.35 × RL	0.65 × RL	RL	3		33.3	33.3
BOOT0	0							RL	3		33.3	33.3
BOOT1	0							RL	3		33.3	33.3
REGEN	0	0.45	RL – 0.45	RL					3	30	33.3	33.3
MSECURE					0	0.35 × RL	0.65 × RL	RL	3		33.3	33.3
I2C.SR.SDA	0	0.4			–0.5	0.3 × RL	0.7 × RL	RL+0.5	3.4	up to 400		
VMODE2					0	0.35 × RL	0.65 × RL	RL	3.4		29.4	29.4
I2C.SR.SCL	0	0.4			–0.5	0.3 × RL	0.7 × RL	RL+0.5	3.4		10	10
I2C.CNTL.SDA	0	0.4			–0.5	0.3 × RL	0.7 × RL	RL+0.5	3.4	up to 400		
I2C.CNTL.SCL	0	0.4			–0.5	0.3 × RL	0.7 × RL	RL+0.5	3.4		10	10

Table 3-4. Digital I/O Electrical Characteristics (continued)

Pin Name	VOL (V)		VOH (V)		VIL (V)		VIH (V)		MAX FREQ (MHz)	MAX LOAD (pF) OUTPUT MODE	MAX RISE[(1)] TIME (ns)	MAX FALL[(1)] TIME (ns)
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
PCM.VCK	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	1	30	100	33
PCM.VDR	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	1	30	100	100
PCM.VDX	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	1	30	100	33
PCM.VFS	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	1	30	33	33
I2S.CLK	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	6.5	30	33	33
I2S.SYNC	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	6.5	30	33	33
I2S.DIN					0	0.35 × RL	0.65 × RL	RL	3.25	30	33	33
I2S.DOUT	0	0.45	RL – 0.45	RL					3.25	30	29	29
DIG.MIC.0					0	0.35 × RL	0.65 × RL	RL	2.4		41.7	41.7
RTSO/ CLD64K.OUT/ BERCLK.OUT	0	0.45	RL – 0.45	RL					3	30	33	33
CTSI/ BERDATA.OUT	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	3	30	33	33
MANU_BRIX	0	0.45	RL – 0.45	RL					3	30	33	33
USBCHRG_ENZ	0	0.3	RL – 0.1	RL					3	30	33	33
USBCHRG_STATZ					0	0.35 × RL	0.65 × RL	RL	3		33	33
CHRG_DET_N	0	0.3	RL – 0.1	RL					3	30	33	33
32KCLKOUT	0	0.45	RL – 0.45	RL					0.032	40	16	16
HFCLKOUT	0	0.45	RL – 0.45	RL					38.4	30	5.0[(2)]	4.7[(2)]
UCLK	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	60	10	1	1
STP GPIO.9	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
DIR GPIO.10	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
NXT GPIO.11	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
DATA0 UART4.TXD	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
DATA1 UART4.RXD	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
DATA2 UART4.RTSI	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
DATA3 UART4.CTSO	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1

Table 3-4. Digital I/O Electrical Characteristics (continued)

Pin Name	VOL (V)		VOH (V)		VIL (V)		VIH (V)		MAX FREQ (MHz)	MAX LOAD (pF) OUTPUT MODE	MAX RISE[(1)] TIME (ns)	MAX FALL[(1)] TIME (ns)
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
GPIO.12	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
DATA4 / GPIO.14	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
DATA5 / GPIO.3	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
DATA6 / GPIO.4	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
DATA7 / GPIO.5	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	30	10	1	1
TEST.RESET					0	0.35 × RL	0.65 × RL	RL	3		33	33
TEST					0	0.35 × RL	0.65 × RL	RL	3	30	29	29
JTAG.TDI/ BERDATA					0	0.35 × RL	0.65 × RL	RL	3		33	33
JTAG.TCK/ BERDATA					0	0.35 × RL	0.65 × RL	RL	3		33	33
GPIO.13 / LEDSYNC	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	3	30	33.3	33.3
GPIO.16	0	0.45	RL – 0.45	RL	0	0.35 × RL	0.65 × RL	RL	3	30	33.3	33.3
DIG.MIC.CLK0	0	0.45	RL – 0.45	RL					2.4	30	41.7	41.7

(1) Min value depends on board conditions, and can be computed with IBIS-models.

(2) Max rise/fall times valid for high drive settings and max load of 20 pF.

4 Clock Specifications

The TPS65951 includes several I/O clock pins. The TPS65951 has two sources of high-stability clock signals: the external high-frequency clock (HFCLKIN) input and an on-board 32-kHz oscillator (optionally, an external 32-kHz signal can be provided). Figure 4-1 shows the clock overview.

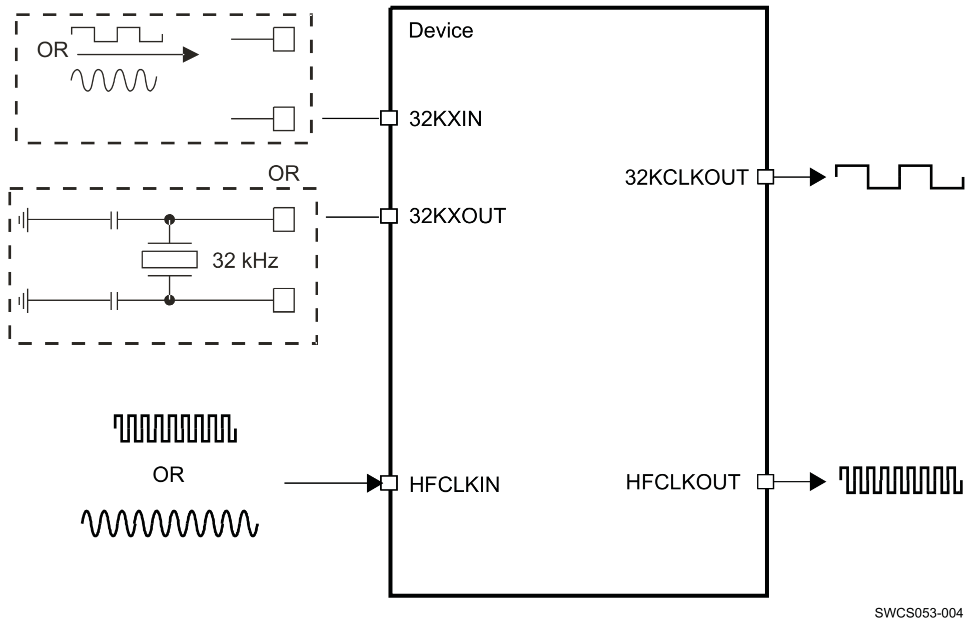


Figure 4-1. Clock Overview

4.1 Features

The TPS65951 accepts two sources of high-stability clock signals:

- 32KXIN/32KXOUT: on-board 32-kHz crystal oscillator (optionally, an external 32-kHz input clock can be provided)
- HFCLKIN: an external high-frequency clock (19.2, 26, or 38.4 MHz)

The TPS65951 has the capability to provide:

- 32KCLKOUT digital output clock
- HFCLKOUT digital output clock with the same frequency as HFCLKIN input clock

4.2 Clock Slicer

Figure 4-2 show the clock slicer block diagram.

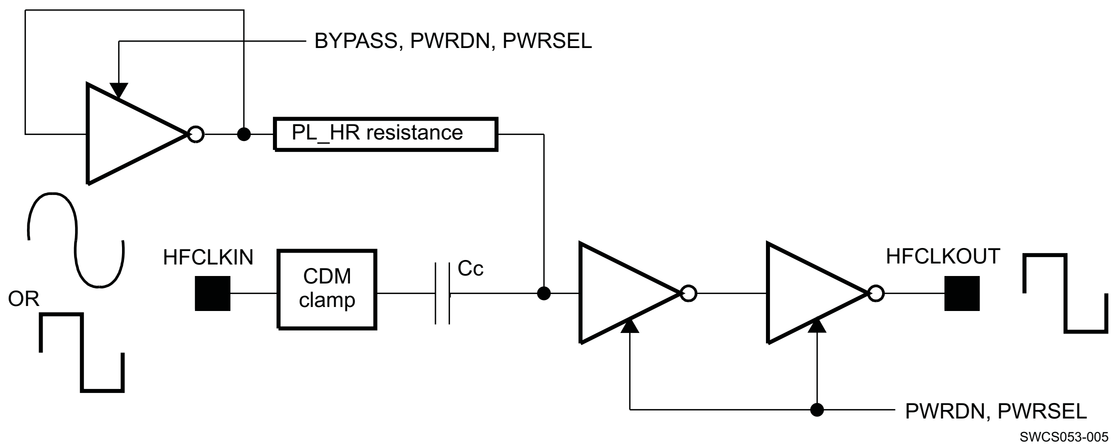


Figure 4-2. Clock Slicer Block Diagram

The clock slicer is disabled by default and enabled when the CLKEN PAD is high. The slicer transforms the HFCLKIN clock input signal into a squared clock signal used internally by the TPS65951 and also outputs it for external use. The HFCLKIN input signal can be:

- A sinusoid with peak-to-peak amplitude varying from 0.3 to 1.45 V
- A square-wave clock signal with maximum amplitude of 1.85 V. In the case of a square-wave clock signal, the slicer will be configured in bypass or power-down mode (see Section 4.2.1).

The HFCLKIN input clock frequency must be 19.2, 26, or 38.4 MHz.

4.2.1 Modes of Operation

There are four different modes programmable by register. By default, the slicer is in a high-performance application mode.

4.2.1.1 Bypass Mode (BP)

In BP mode which overrides all the other modes, the input signal is directly connected to the output through some buffers. The input is a rail-to-rail square wave.

4.2.1.2 Power-Down Mode (PD)

During PD mode if bypass mode is not active, the cell does not consume any current if bypass mode is not active.

4.2.1.3 Low-Power Application Mode (LP)

In LP mode, the input sine wave is converted to a CMOS signal (square wave) with low-power consumption.

4.2.1.4 High-Performance Application Mode (HP)

In HP mode, the input sine wave is converted to a CMOS signal (square wave). It has lower duty cycle degradation and input-to-output delay in comparison to the low-power mode, but it consumes more current. The drive of the squaring inverter is increased by connecting additional inverters in parallel. Details can be found in the clock slicer electrical characteristics table (see Table 4-1).

4.2.2 Clock Slicer Electrical Characteristics

Table 4-1 summarizes the clock slicer electrical characteristics.

Table 4-1. Clock Slicer Electrical Characteristics

PARAMETER	MODE	MIN	TYP	MAX	UNIT
Input frequency		10	26	40	MHz
Input dynamic range	LP / HP	0.3	0.7	1.45	V_{PP}
	BP / PD	0		1.85 (1)	
Harmonic content of input signal (with 0.7-V_{PP} amplitude): 2nd component	LP / HP			–25	dBc
Input clock signal duty cycle		40%		60%	
Internal coupling capacitor		4.2	5	5.7	pF
Parallel input resistance over 10 to 40 MHz range	LP	15		60	kΩ
	HP	30		75	kΩ
	BP / PD	1		100	MΩ
Parallel input capacitance over 10 MHz to 40 MHz range	LP	0.3		0.8	pF
	HP	0.3		0.7	
	BP / PD	0.08		1	
Output duty cycle with V_{IN} = 0.2 V_{PP}	LP / HP	40%	50%	60%	
Propagation delay	LP	4		18	ns
	HP	3		15	
	BP / PD	0.2		3	
Power supply rejection ratio sideband (1% RMS of supply voltage added sine 5 MHz)	LP / HP	26			dBc
Current consumption at maximum input of 40 MHz	LP			175	µA
	HP			235	µA
	BP / PD			39	nA
Power-up time	LP / HP			1	ms
Output peak-to-peak jitter with an input peak-to-peak jitter < 0.1% and for jitter frequency below 300 kHz	LP / HP			0.2%	
Output peak-to-peak jitter with an input peak-to-peak jitter < 0.1% and for jitter frequency above 300 kHz	LP / HP			1%	

(1) Bypass input maximum voltage is the same as the maximum voltage provided for the I/O interface.

4.3 Input Clock Specifications

The clock system accepts two input clock sources:

- 32-kHz crystal oscillator clock or sinusoidal/squared clock
- HFCLKIN high frequency input clock

4.3.1 Clock Source Requirements

Table 4-2 summarizes the input clock requirements.

Table 4-2. TPS65951 Input Clock Source Requirements

PAD	CLOCK FREQUENCY		STABILITY	DUTY CYCLE
32KXIN 32KXOUT	32.768 kHz	Crystal	±30 ppm	40% / 60%
		Square wave	–	45% / 55%
		Sine wave	–	–
HFCLKIN	19.2 MHz, 26 MHz, 38.4 MHz	Square wave	±150 PPM	45% / 55%
		Sine wave	–	–

4.3.2 High Frequency Input Clock

HFCLKIN stands for high frequency input clock. It can be either a square- or a sine-wave input clock. If a square-wave input clock is provided, it is recommended to switch the block to bypass mode when possible to avoid loading the clock (see Section 4.2).

Figure 4-3 shows the HFCLKIN clock distribution.

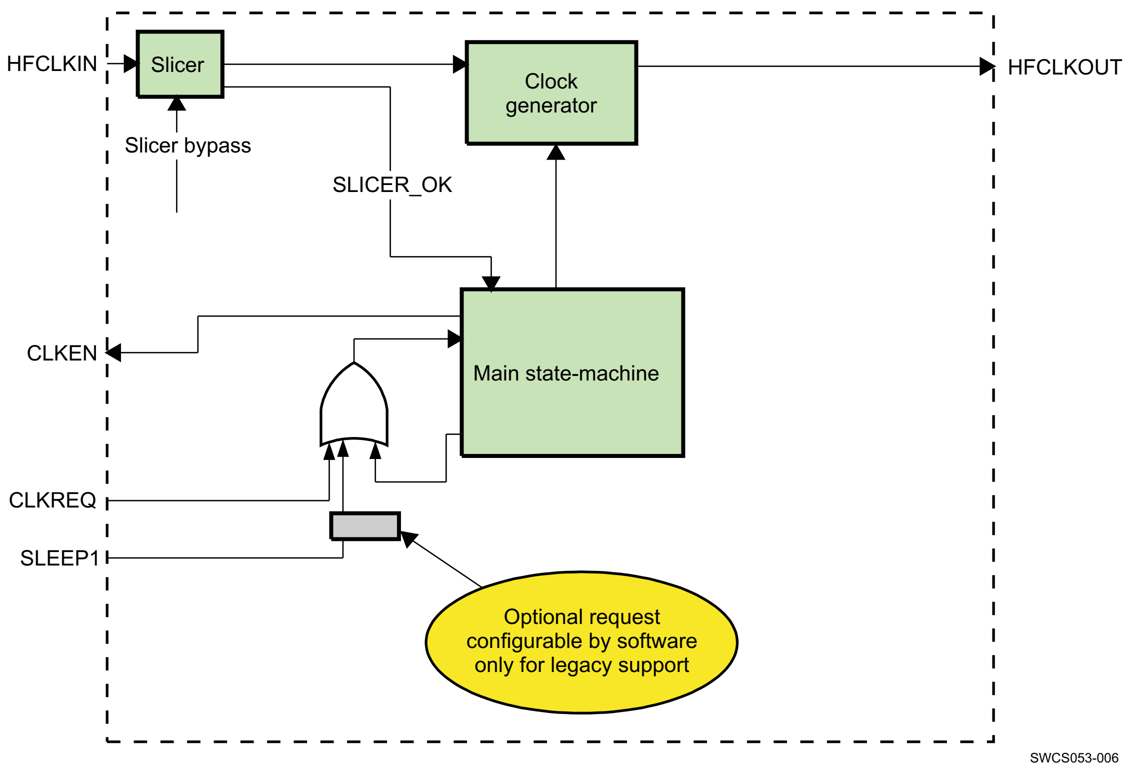


Figure 4-3. HFCLKIN Clock Distribution

When a device needs a clock signal other than 32.768 kHz, it makes a clock request and activates the CLKREQ pin. As a result, the TPS65951 immediately sets CLKEN to 1 to warn the clock provider in the system about the clock request. Then, the TPS65951 opens a gated clock and a high-frequency output clock signal is available through the HFCLKOUT pin. The output drive of HFCLKOUT is programmable (low drive (MISC_CFG[CLK_HF_DRV] = 0) max load 20 pF, high drive (MISC_CFG[CLK_HF_DRV] = 1) maximum load 30 pF), by default it is programmed to support low drive.

CLKREQ has a weak pulldown resistor to support the wired-OR clock request.

Figure 4-4 shows an example of the wired-OR clock request.

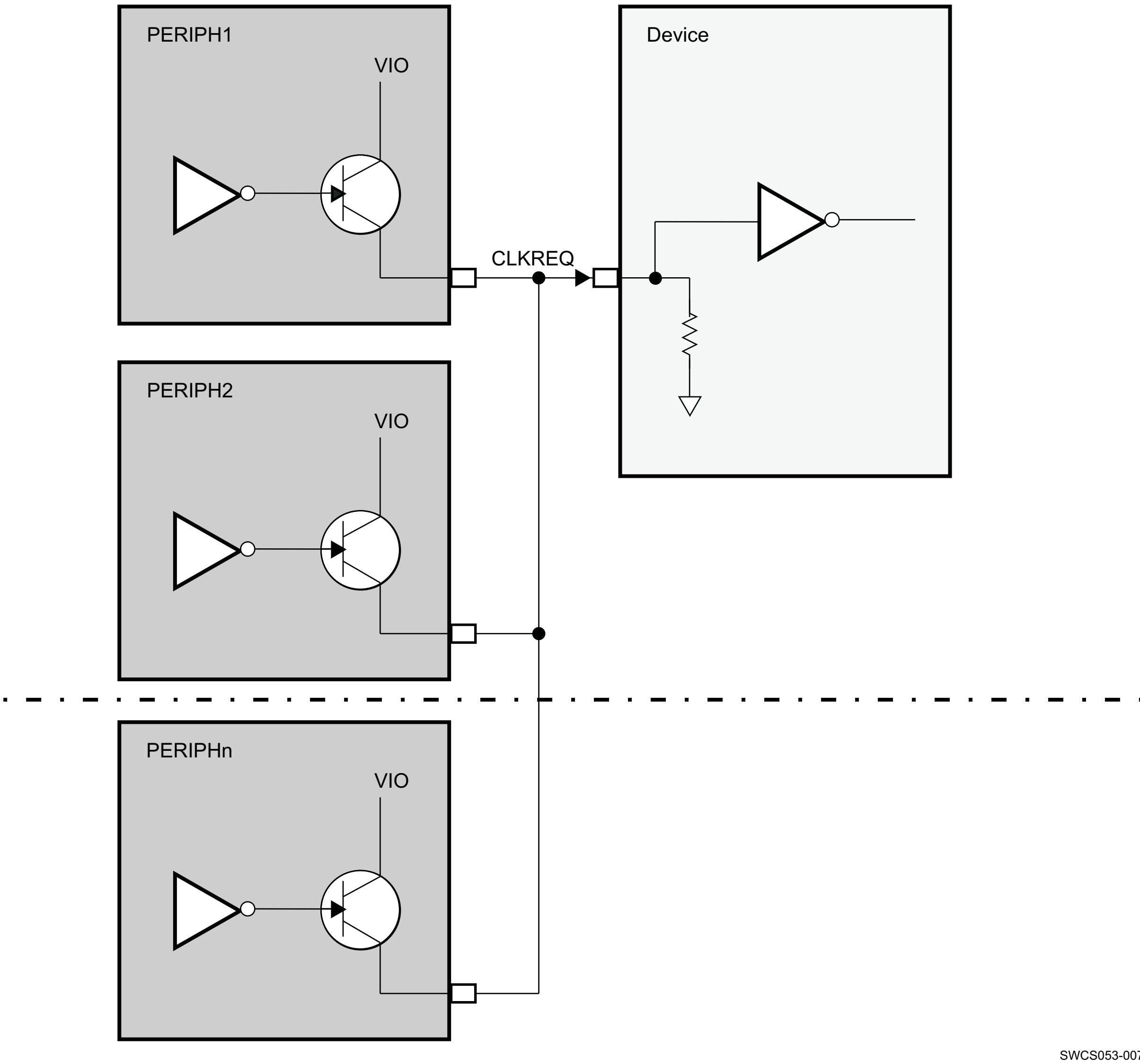


Figure 4-4. Example of Wired-OR Clock Request

Note that the timer default value must be the worst case (10 ms) for the clock providers. For legacy or workaround support, the signal NSLEEP1 can also be used as a clock request even if it is not its primary goal. By default, this feature is disabled and must be enabled individually by setting the register bits associated with each signal.

Table 4-3 details the input clock electrical characteristics of the HFCLKIN input clock.

Table 4-3. HFCLKIN Input Clock Electrical Characteristics

	PARAMETER DESCRIPTION	CONFIGURATION MODE SLICER	MIN	TYP	MAX	UNIT
	Frequency			19.2, 26, or 38.4		MHz
	Start-up time	LP / HP (sine wave)			4	μs
	Input dynamic range	LP / HP (sine wave)	0.3	0.7	1.45	V_{PP}
		BP / PD (square wave)	0		1.85 (1)	
	Current consumption	LP			175	μA
		HP			235	
		BP / PD			39	nA
	Harmonic content of input signal (with 0.7-V_{PP} amplitude): 2nd component	LP / HP (sine wave)			–25	dBc
V_{IH}	Voltage input high (1)	BP (square wave)	0.65 × IO.1P8			V
V_{IL}	Voltage input low (1)	BP (square wave)			0.35 × IO.1P8	V

(1) Bypass input max voltage is the same as the maximum voltage provided for the I/O interface (IO.1P8V).

Table 4-4 details the input clock timing requirements of the HFCLKIN input clock when the source is a square wave.

Table 4-4. HFCLKIN Square Input Clock Timing Requirements with Slicer in Bypass

NAME	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
CH0	$1/t_{C(HFCLKIN)}$	Frequency, HFCLKIN		19.2, 26, or 38.4		MHz
CH1	$t_{W(HFCLKIN)}$	Pulse duration, HFCLKIN low or high	0.45 × $t_{C(HFCLKIN)}$		0.55 × $t_{C(HFCLKIN)}$	ns
CH3	$t_{R(HFCLKIN)}$	Rise time, HFCLKIN	0		5	ns
CH4	$t_{F(HFCLKIN)}$	Fall time, HFCLKIN	0		5	ns

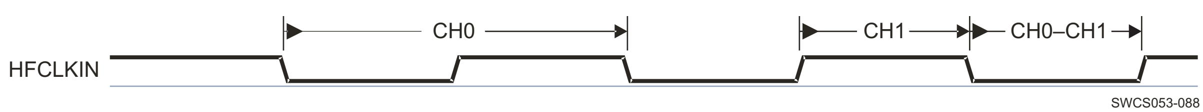


Figure 4-5. HFCLKIN Squared Input Clock

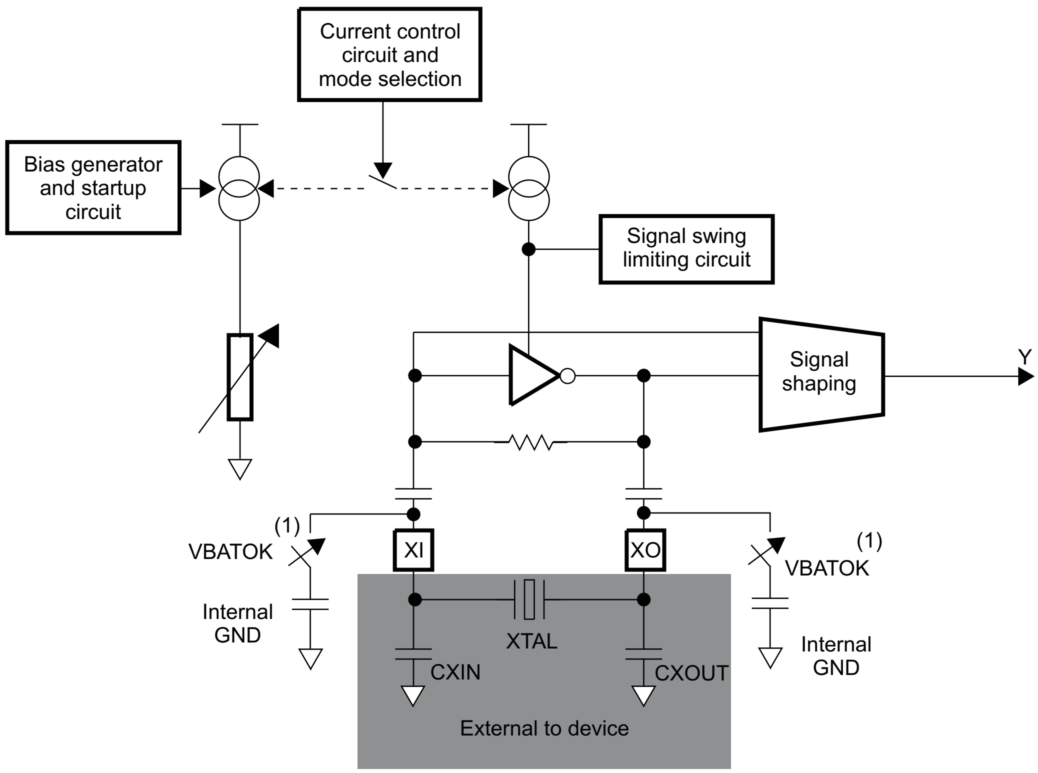
4.3.3 32-kHz Input Clock

A 32.768-kHz input clock (often abbreviated to 32-kHz) generates the clocks for the RTC. It has a low-jitter mode where the current consumption increases for lower jitter. It is possible to use the 32-kHz input clock with either an external crystal or clock source. Depending on the mode chosen, the 32K oscillator is configured as being either:

- An external 32.768-kHz crystal through the 32KXIN/32KXOUT balls (see Figure 4-6). This configuration is available for the master mode only (for more details, see Section 7).
- An external square/sine wave of 32.768 kHz through 32KXIN with amplitude equal to 1.8 or 1.85 V (see Figure 4-8, Figure 4-9). This configuration is available for the master and slave modes (for more details, see Section 7).

4.3.3.1 External Crystal Description

Figure 4-6 shows the 32-kHz oscillator block diagram with crystal in master mode.



NOTE: Switches close by default and open only if register access enables the very-low-power mode when VBAT < 2.7 V.

Figure 4-6. 32-kHz Oscillator Block Diagram In Master Mode With Crystal

CXIN and CXOUT represent the total capacitance of the PCB and components, excluding the crystal. Their values depend on the datasheet of the crystal, also the internal capacitors and the parallel capacitor. The frequency of the oscillations depends on the value of the capacitors. The crystal must be in the fundamental mode of operation and parallel resonant.

NOTE

For the values of CXIN and CXOUT, see Table 12-1, *TPS65951 External Components*.

Table 4-5 summarizes the required electrical constraints.

Table 4-5. Crystal Electrical Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Parallel resonance crystal frequency		32.768		kHz
Input voltage, Vin (normal mode)	1.0	1.3	1.55	V
Internal capacitor on each input (Cint)	8	10	12	pF
Parallel input capacitance (Cpin)			1	pF
Nominal load cap on each oscillator input CXIN and CXOUT(1)	CXIN = CXOUT = Cosc × 2 – (Cint + Cpin)			pF
Pin to pin capacitance		1.6	1.8	pF

(1) Nominal load capacitor on each oscillator input defined as CXIN = CXOUT = Cosc × 2 – (Cint + Cpin). Cosc is the load capacitor defined in the crystal oscillator specification, Cint is the internal capacitor, and Cpin is the parallel input capacitor.

Table 4-5. Crystal Electrical Characteristics (continued)

PARAMETER	MIN	TYP	MAX	UNIT
Crystal ESR(2)			90	kΩ
Crystal shunt capacitance, C_O			1	pF
Crystal tolerance at room temperature, 25°C	–30		30	ppm
Crystal tolerance versus temperature range (–40°C to 85°C)	–200		200	ppm
Maximum drive power			1	µW
Operating drive level			0.5	µW
Crystal quality factor	13k		54k	

(2) The crystal motional resistance Rm relates to the equivalent series resistance (ESR) by the following formula:

$$ESR = R_m\left(1 + \frac{C_O}{C_L}\right)^2$$

SWCS053-e001

Measured with the load capacitance specified by the crystal manufacturer. In fact, if CXIN = CXOUT = 10 pF, then C_L = 5 pF. Parasitic capacitance from the package and board must also be taken in account.

When selecting a crystal, the system designer must consider the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 4-6 and Table 4-7 list the switching characteristics of the oscillator and the input requirements of the 32.768-kHz input clock. Figure 4-7 shows the crystal oscillator output in normal mode.

Table 4-6. Base Oscillator Switching Characteristics

NAME	PARAMETER DESCRIPTION		MIN	TYP	MAX	UNIT
f_P	Oscillation frequency			32.768		kHz
t_{SX}	Start-up time, all conditions				500	ms
	Start-up tine, 25°C				360	
I_{DDA}	Active current consumption (configured through LOJIT register bit)	High jitter mode			1.8	µA
		Low jitter mode			8	
I_{DDQ}	Current consumption	Low battery mode (1.2 V)			1	µA
		Startup			8	

Table 4-7. 32-kHz Crystal Input Clock Timing Requirements

NAME	PARAMETER DESCRIPTION		MIN	TYP	MAX	UNIT
OC0	$1/t_{C(32KHZ)}$	Frequency, 32 kHz		32.768		kHz
OC1	$t_{W(32KHZ)}$	Pulse duration, 32 kHz low or high	$0.40 \times t_{C(32KHZ)}$		$0.60 \times t_{C(32KHZ)}$	µs

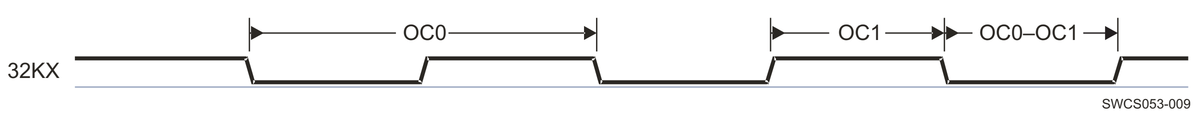


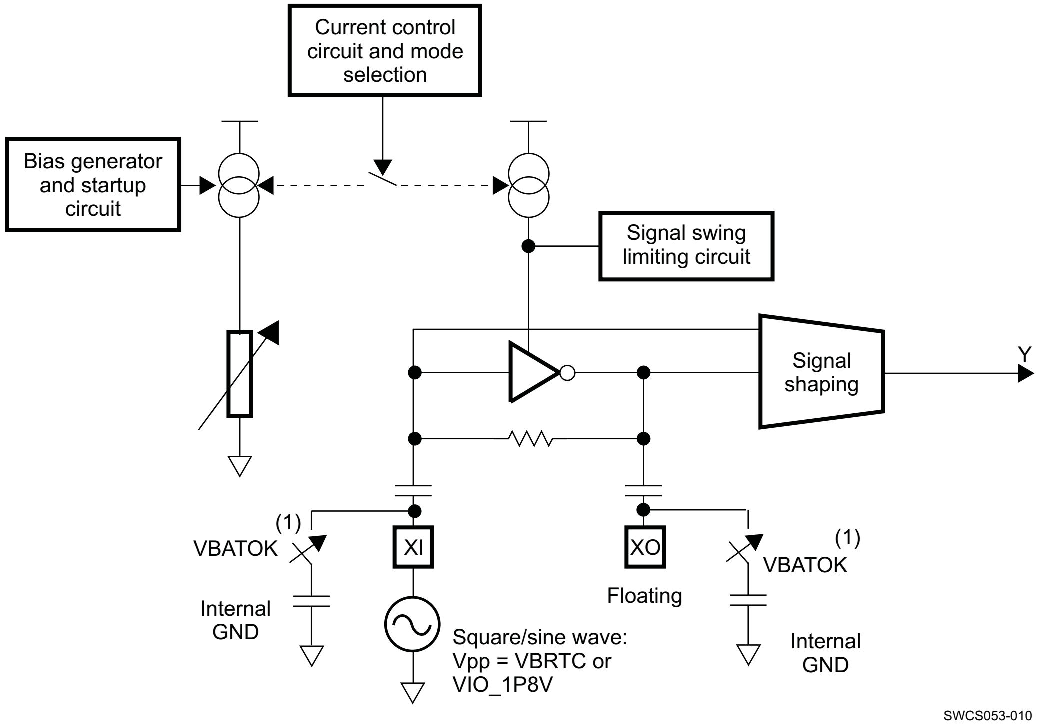
Figure 4-7. 32-kHz Crystal Input

4.3.3.2 External Clock Description

Figure 4-8 shows the 32-kHz oscillator block diagram with a 32.768-kHz square- or sine-wave signal in master and slave modes. Figure 4-9 shows an external clock source when the oscillator is configured in bypass mode. Thus, there are two configurations:

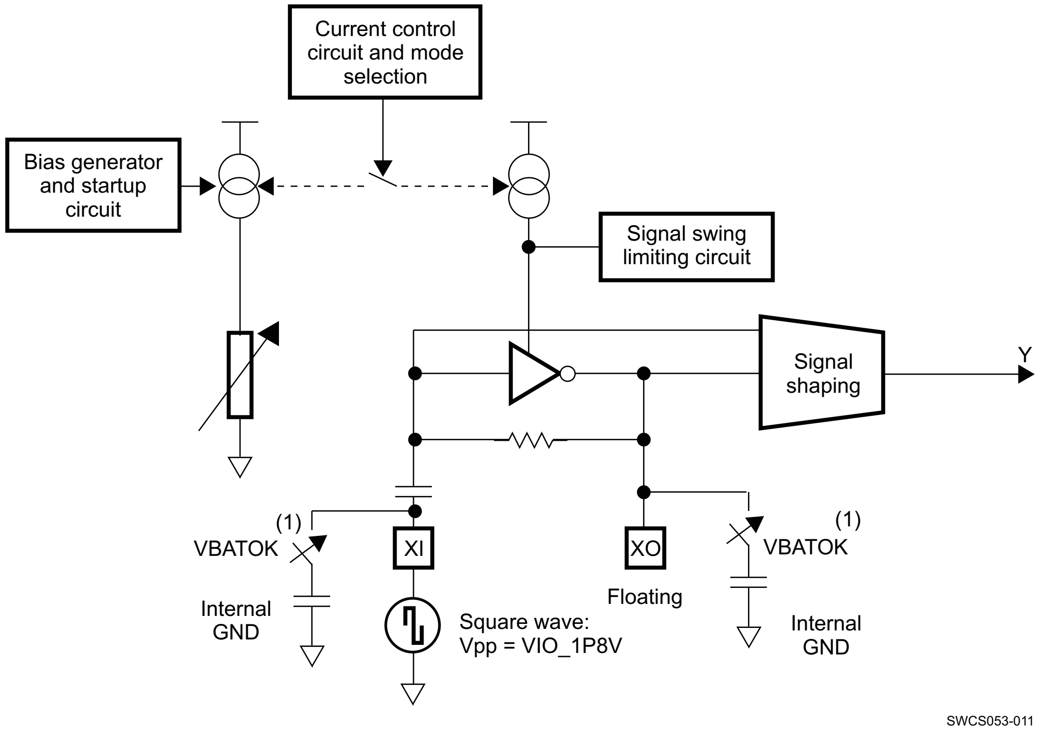
- A square- or sine-wave input can be applied to the 32KXIN pin with amplitude of 1.85 or 1.8 V. The 32KXOUT pin can be left floating. This configuration, showed in Figure 4-8, is used if no charge is applied on the 32KXOUT pin.

- The oscillator is in bypass mode and a square-wave input can be applied to the 32KXIN pin with amplitude of 1.8 V. The 32KXOUT pin can be left floating. This configuration, shown in Figure 4-9, is used if the oscillator is in bypass mode.



(1) Switches close by default and open only if register access enables the very-low-power mode when VBAT < 2.7 V.

Figure 4-8. 32-kHz Oscillator Block Diagram Without Crystal Option 1



(1) Switches close by default and open only if register access enables the very-low-power mode when VBAT < 2.7 V.

Figure 4-9. 32-kHz Oscillator in Bypass Mode Block Diagram Without Crystal Option 2

Table 4-8 summarizes the electrical constraints required by the 32-kHz input square- or sine-wave clock used:

Table 4-8. 32-kHz Input Square- or Sine-wave Clock Source Electrical Characteristics

NAME	PARAMETER DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		32.768		kHz
C_I	Input capacitance	28	35	42	pF
C_{FI}	On-chip foot capacitance to GND on each input (see Figure 4-8, Figure 4-9)	8	10	12	pF
V_{PP}	Square-/sine-wave amplitude in bypass mode or not		1.5[(1)]		V
V_{IH}	Voltage input high, square wave in bypass mode[(1)]	0.65 × VBRTC			V
V_{IL}	Voltage input low, square wave in bypass mode[(2)]			0.35 × VBRTC	V

(1) Bypass input max voltage is the same as the maximum voltage provided for the I/O interface. The input buffer is supplied by VBRTC, but it is supported up to IO.1P8. Because the input buffer is supplied VBRTC, VIH and VIL are relative to VBRTC.
(2) Bypass input max voltage is the same as the maximum voltage provided for the I/O interface. The input buffer is supplied by VBRTC, but it is supported up to IO.1P8. Because the input buffer is supplied VBRTC, VIH and VIL are relative to VBRTC.

Table 4-9 details the input requirements of the 32-kHz square-wave input clock.

Table 4-9. 32-kHz Square-wave Input Clock Source Timing Requirements

NAME	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
CK0	$1/t_{C(32KHZ)}$	Frequency, 32 kHz		32.768		kHz
CK1	$t_{W(32KHZ)}$	Pulse duration, 32 kHz low or high	0.45 × $t_{C(32KHZ)}$		0.55 × $t_{C(32KHZ)}$	μs
CK3	$t_{R(32KHZ)}$	Rise time, 32 kHz[(1)]			0.1 × $t_{C(32KHZ)}$	μs
CK4	$t_{F(32KHZ)}$	Fall time, 32 kHz[(1)]			0.1 × $t_{C(32KHZ)}$	μs

(1) The capacitive load is equivalent to 30 pF.

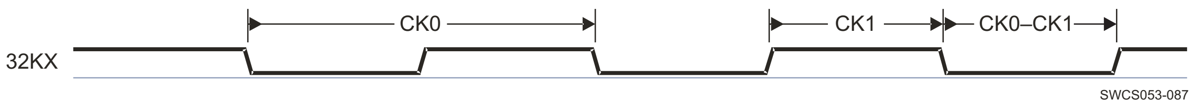


Figure 4-10. 32-kHz Square- or Sine-Wave Input Clock

4.4 Output Clock Specifications

The TPS65951 device provides two output clocks:

- 32KCLKOUT
- HFCLKOUT

4.4.1 32KCLKOUT Output Clock

Figure 4-11 shows the block diagram for the 32.768-kHz clock output.

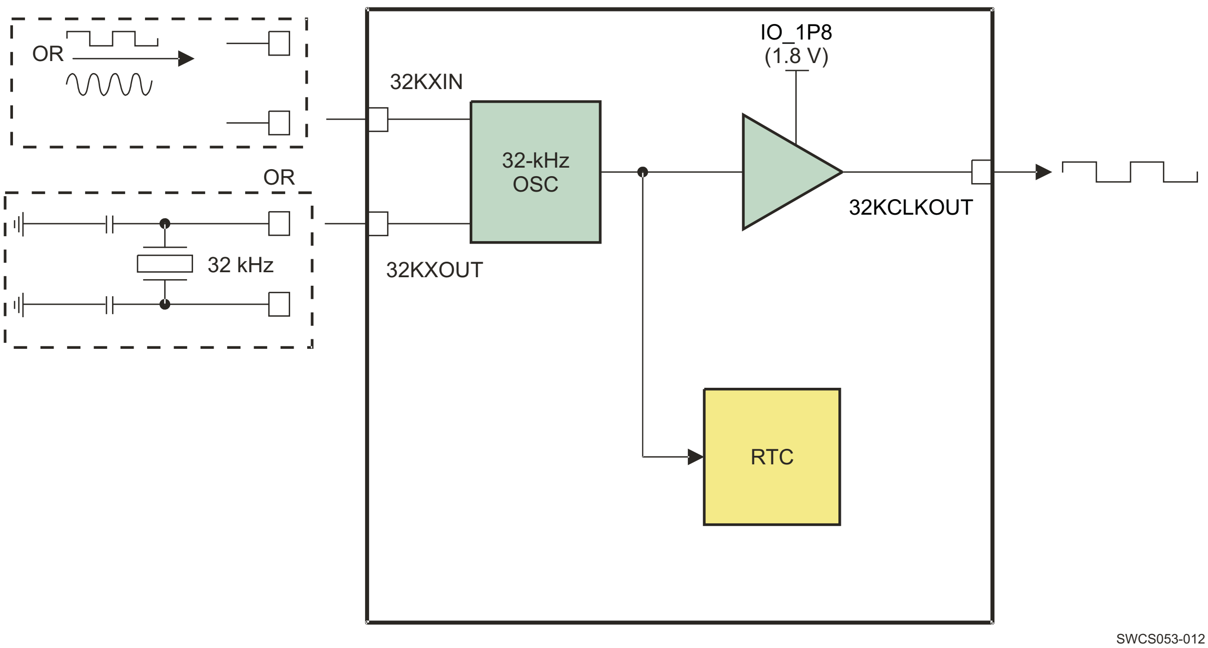


Figure 4-11. 32.768-kHz Clock Output Block Diagram

The TPS65951 device has an internal 32.768-kHz oscillator connected to either an external 32.768-kHz crystal through the 32KXIN/32KXOUT balls or an external digital 32.768-kHz clock through the 32KXIN input (see Figure 4-11). The TPS65951 device also generates a 32.768-kHz digital clock through the 32KCLKOUT pin and can broadcast it externally to the application processor or any other devices. The 32KCLKOUT clock is broadcast by default in the TPS65951 ACTIVE state.

The 32.768-kHz clock (or signal) is also used to clock the RTC (real-time clock) embedded in the TPS65951. The RTC is not enabled by default. It is up to the host processor to set the correct date and time and to enable the RTC functionality.

The 32KCLKOUT output buffer can drive several devices (up to 40-pF load). At start-up, the 32.768-kHz output clock (32KCLKOUT) must be stabilized (frequency/duty cycle) prior to the signal output (description in TRM 3.3.2.2 32-kHz Oscillator Stabilization).

Table 4-10 summarizes the output clock electrical characteristics.

Table 4-10. 32KCLKOUT Output Clock Electrical Characteristics

NAME	PARAMETER DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		32.768		kHz
C_L	Load capacitance			40	pF
V_{OUT}	Output clock voltage, depending on output reference level IO.1P8 (see Section 2)		1.8 (1)		V
V_{OH}	Voltage output high	V_{OUT} – 0.45		V_{OUT}	V
V_{OL}	Voltage output low	0		0.45	V

(1) The output voltage depends on output reference level which is IO.1P8 (see Section 2, *Terminal Description*).

Table 4-11 details the output clock timing characteristics. Figure 4-12 shows the 32KCLKOUT output clock waveform.

Table 4-11. 32KCLKOUT Output Clock Switching Characteristics

NAME	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
CK0	$1/t_{C(32KCLKOUT)}$	Frequency		32.768		kHz
CK1	$t_{W(32KCLKOUT)}$	Pulse duration, 32KCLKOUT low or high	0.40 × $t_{C(32KCLKOUT)}$		0.60 × $t_{C(32KCLKOUT)}$	ns
CK2	$t_{R(32KCLKOUT)}$	Rise time, 32KCLKOUT (1)	4		16	ns
CK3	$t_{F(32KCLKOUT)}$	Fall time, 32KCLKOUT (1)	4		16	ns
	SSB Phase Noise	At 1-kHz offset from the carrier			–110	dBc/Hz

(1) The output capacitive load is equivalent to 30 pF.

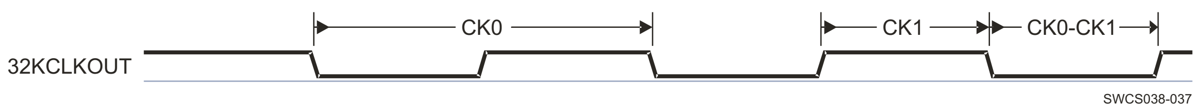


Figure 4-12. 32KCLKOUT Output Clock

4.4.2 *HFCLKOUT Output Clock*

Table 4-12 summarizes the HFCLKOUT output clock electrical characteristics (for more information, see Section 4.2).

Table 4-12. HFCLKOUT Output Clock Electrical Characteristics

NAME	PARAMETER DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency	19.2, 26, or 38.4			MHz
C_L	Load capacitance			30	pF
V_{OUT}	Output clock voltage, depending on output reference level IO.1P8 (see Section 2)		1.8 (1)		V
V_{OH}	Voltage output high	V_{OUT} – 0.45		V_{OUT}	V
V_{OL}	Voltage output low	0		0.45	V

(1) The output voltage depends on output reference level which is IO.1P8 (see Section 2).

Table 4-13 details the HFCLKOUT output clock timing characteristics.

Table 4-13. HFCLKOUT Output Clock Switching Characteristics

NAME	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
CHO1	$1/t_{C(HFCLKOUT)}$	Frequency	19.2, 26, or 38.4			MHz
CHO2	$t_{W(HFCLKOUT)}$	Pulse duration, HFCLKOUT low or high	0.40 × $t_{C(HFCLKOUT)}$		0.60 × $t_{C(HFCLKOUT)}$	ns

Table 4-13. HFCLKOUT Output Clock Switching Characteristics (continued)

NAME	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
CHO3	$t_{R(HFCLKOUT)}$	Rise time, HFCLKOUT, Low Drive (1)				ns
		Load: 5 pF	0.5		3.8	
		Load: 10 pF	1		5.5	
		Rise time, HFCLKOUT, High Drive (2)				
		Load: 10 pF	0.5		2.9	
		Load: 20 pF	1		5.0	
CHO4	$t_{F(HFCLKOUT)}$	Fall time, HFCLKOUT, Low Drive (1)				ns
		Load: 5 pF	0.5		3.5	
		Load: 10 pF	1		5.1	
		Rise time, HFCLKOUT, High Drive (2)				
		Load: 10 pF	0.5		2.7	
		Load: 20 pF	1		4.7	

(1) Low Drive: MISC_CFG[CLK_HF_DRV] = 0 (default)
(2) High Drive: MISC_CFG[CLK_HF_DRV] = 1

Figure 4-13 shows the HFCLKOUT output clock waveform and Figure 4-15 shows the HFCLKOUT behavior.

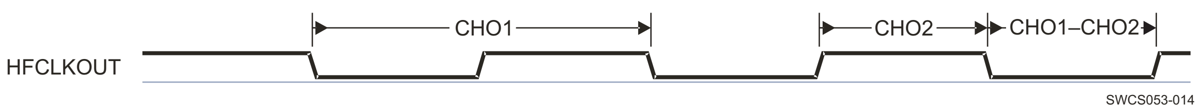
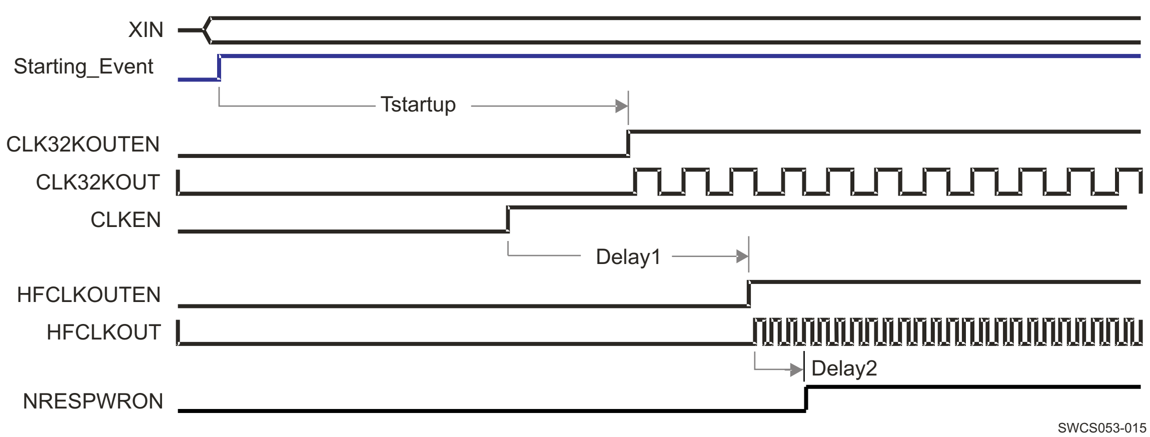


Figure 4-13. HFCLKOUT Output Clock

4.4.3 *Output Clock Stabilization Time*

Figure 4-14 shows the 32KCLKOUT and HFCLKOUT clock stabilization time.



NOTE: Tstartup, Delay1, Delay2, Delay3 depend on the boot mode (see Section 6.5, *Power Management*)

Figure 4-14. 32KCLKOUT and HFCLKOUT Clock Stabilization Time

In Figure 4-15, HFCLKIN is the input signal of the clock slicer coming from an external source. HFCLKOUT is the output of the clock slicer; a squared clock signal that is present after the propagation delay of the clock slicer (for numerical values, see Table 4-1).

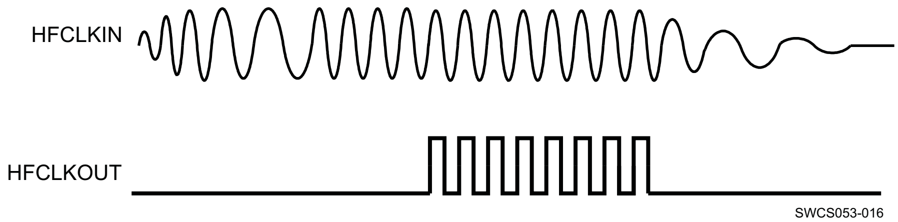


Figure 4-15. HFCLKOUT Behavior

5 Audio/Voice Module

Figure 5-1 shows the audio/voice module block diagram.

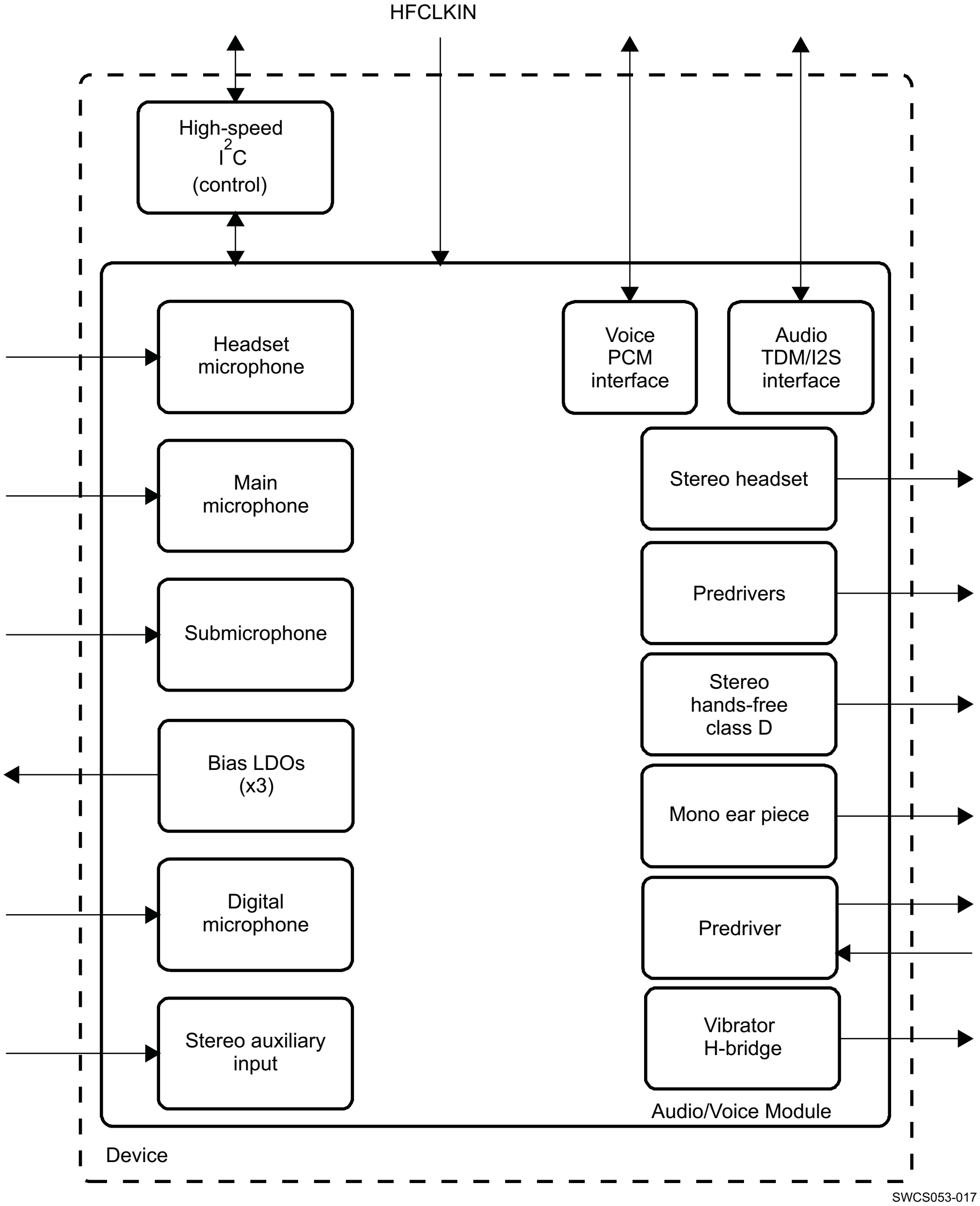


Figure 5-1. Audio/Voice Module Block Diagram

5.1 Audio/Voice Downlink (RX) Module

The audio/voice module includes the following output stages:

- Mono/stereo single-ended headset amplifier
- Stereo differential integrated class D 8-Ω hands-free amplifiers
- Predrivers output signals for external class D amplifiers (single-ended)
- Mono differential earpiece amplifier
- Vibrator H-bridge

All output stages of the downlink (except Class-D of the Hands-Free) are powered by VINTANA2. Characteristics are given for a VBAT higher than 3.0 V (involving VINTANA2 output level equal 2.75 V). When VBAT is in the range of 2.7 to 3.0 V (VINTANA2 = 2.5 V), only functionality is ensured.

5.1.1 Earphone Output

5.1.1.1 Earphone Output Characteristics

Analog signals from the audio and/or voice interface are fed to the earphone amplifier. This amplifier with different gains provides a full differential signal on terminals EARP and EARM. Figure 5-2 shows the earphone amplifier. Table 5-1 summarizes the earphone output characteristics.

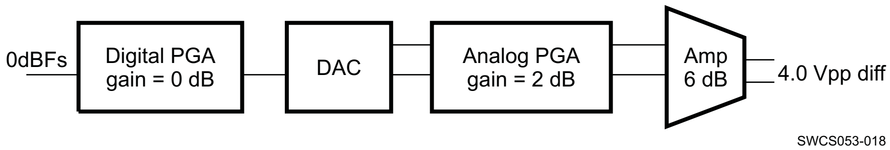


Figure 5-2. Earphone Amplifier

Table 5-1. Earphone Amplifier Output Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential load impedance		26	32		Ω
		0	100		pF
Gain range (1)	Audio path	–86		36	dB
	Voice path	–60		36	
Absolute gain error		–1		1	dB
Gain variation with frequency	F = 20 Hz to 20 kHz (Audio path, Fs = 48 kHz, 44. 1 kHz)	–0.5		0.5	dB
Maximum output power	At 1.4 Vrms differential output voltage Load impedance = 32 Ω			69	mW
Peak-to-peak differential output voltage (0 dBFs)	Load impedance = 32 Ω Default gain (2)	3.66		4.22	V_{PP}
Total harmonic distortion Default gain (2) Load impedance = 32 Ω	At 0 dBFs		–65	–60	dB
	At –6 dBFs		–70	–65	
	At –20 dBFs			–60	
	At –60 dBFs			–30	
Signal Noise Ratio (20 Hz to 20 kHz, A-weighted)	Gain = 0 dB Load = 32 Ω	80	87		dB
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Gain = 0 dB Load = 32 Ω		–90	–85	dBFs
			42	75	uVrms
Output PSRR (for all gains)	20 Hz to 4 kHz	80	90		dB
(Input signal: 1-kHz sine, 600 mVpp GSM ripple at 217 Hz with 10 µs rise/fall times, at 12.5% duty-cycle)	20 Hz to 20 kHz	62	70		

(1) Audio digital filter = –62 dB to 0 dB (1-dB step) and 0 dB to 12 dB (6-dB step)
Voice digital filter = –36 dB to 12 dB (1-dB step)
ARXPGA (volume control) = –24 dB to 12 dB (2-dB steps)
Output driver = 0 dB, 6 dB, 12 dB

(2) The default gain setting assumes the ARXPGA has 2-dB gain setting (volume control) and output driver at 6-dB gain setting.

5.1.1.2 External Components and Application Schematics

Figure 5-3 shows a simplified earphone speaker schematic.

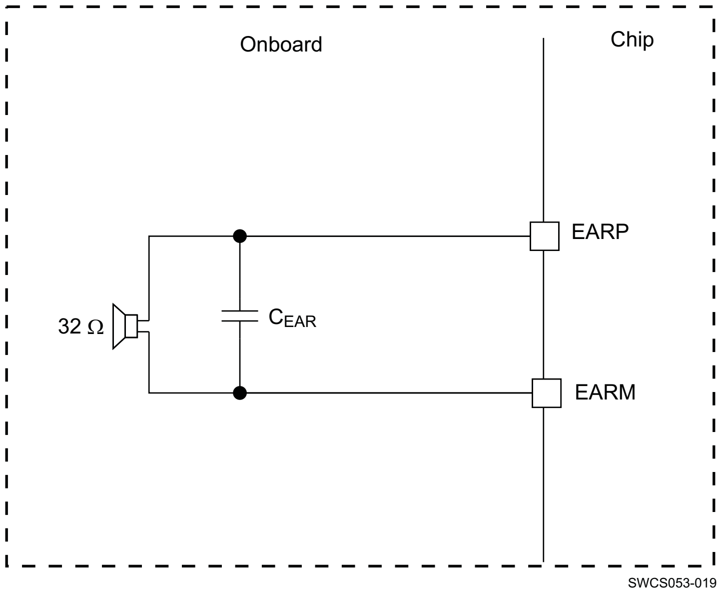


Figure 5-3. Earphone Speaker

NOTE

For the component values, see Table 12-1, *TPS65951 External Components*.

5.1.2 8-Ω Stereo Hands-Free

The digital signal from the audio and/or voice interface is fed to two class D amplifiers. These 8-Ω speaker amplifiers provide a stereo differential signal on terminal pairs (IHF.RIGHT.P, IHF.RIGHT.M) and (IHF.LEFT.P, IHF.LEFT.M).

5.1.2.1 8-Ω Stereo Hands-Free Output Characteristics

Figure 5-4 shows the 8-Ω stereo hands-free amplifier. Table 5-2 summarizes the 8-Ω stereo hands-free output characteristics.

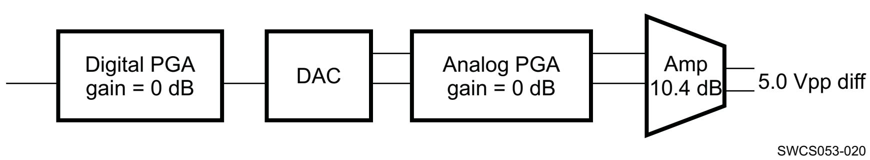


Figure 5-4. 8-Ω Stereo Hands-Free Amplifiers

Table 5-2. 8-Ω Stereo Hands-Free Output Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBAT voltage		3.0	3.6	4.6	V
Load impedance		6	8	32	Ω
Gain range(1)	Audio path	–75.6		34.4	dB
	Voice path	–49.6		34.4	
Absolute gain error		–1		1	dB
Gain variation with frequency	F = 20 Hz to 20 kHz (Audio path, Fs = 48 kHz, 44.1 kHz)	–0.5		0.5	dB
Maximum output power (load impedance = 8 Ω)	VBAT > 3.6 V		400		mW
	VBAT > 4.0 V		700		
Peak-to-peak differential output voltage	VBAT > 3.6 V (0 dBFs)	4.45	5.0	5.6	V_{PP}
	VBAT > 4.0 V (2 dBFs)	5.57	6.25	7	
Total harmonic distortion (load impedance = 8 Ω, gain setting = 0 dB) (VBAT > 3.6 V)	At 0 dBFs		–60	–40	dBFs
	At –10 dBFs			–60	
	At –20 dBFs			–45	
	At –60 dBFs			–20	
Total harmonic distortion (load impedance = 8 Ω, (VBAT > 4.2 V)	2 dBFs		–60	–40	dB
Idle channel noise (20 Hz to 20 kHz, A-weighted)	0 dB gain		–88		dBFs
PSRR (input signal 1 kHz sine, 300 mVPP GSM ripple at 217 Hz with 10-μs rise/fall times, at 12.5% duty cycle)	From VBAT	75	80		dB
Efficiency	Power on load = 400 mW Load impedance = 8 Ω	70%			
Power dissipation	Power on load = 400 mW Load impedance = 8 Ω			175	mW
Idle current consumption on VBAT	Without input signal		6		mA
Clock frequency for the ramp generation		384		426.6	kHz
I_{DDQ} current	At 25°C		0.6		μA

(1) Audio digital filter = –62 dB to 0 dB (1-dB step) and 0 dB to 12 dB (6-dB step)
Voice digital filter = –36 dB to 12 dB (1-dB step)
ARXPGA (volume control) = –24 dB to 12 dB (2-dB steps)
Output driver = 10.4 dB

5.1.2.1.1 Short-Circuit Protection

There is short-circuit protection for hands-free amplifiers to limit power dissipation to 1.2 W. The short-circuit protection can be disabled by register (PMBR2[3], CLASSD_SCD_DIS).

- CLASSD_SCD_DIS = 0 (default): Class-D short-circuit protection is enabled. If a short-circuit is detected, the short-circuit detection block switches off the hands-free speakers output stages. A software restart is needed to restart the Class-D. No interruption is generated.
- CLASSD_SCD_DIS = 1: Class-D short-circuit detection is disabled.

The scenario of a short-circuit is as follows:

- Output load terminals
- Output load and ground
- Output load and battery

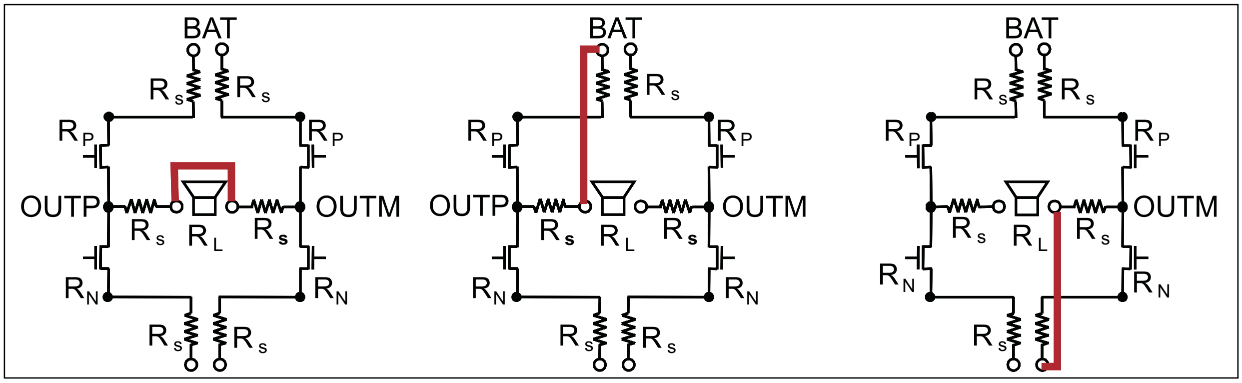


Figure 5-5. Class-D: Short-Circuits

5.1.2.2 External Components and Application Schematics

Figure 5-6 shows a simplified 8-Ω stereo hands-free schematic.

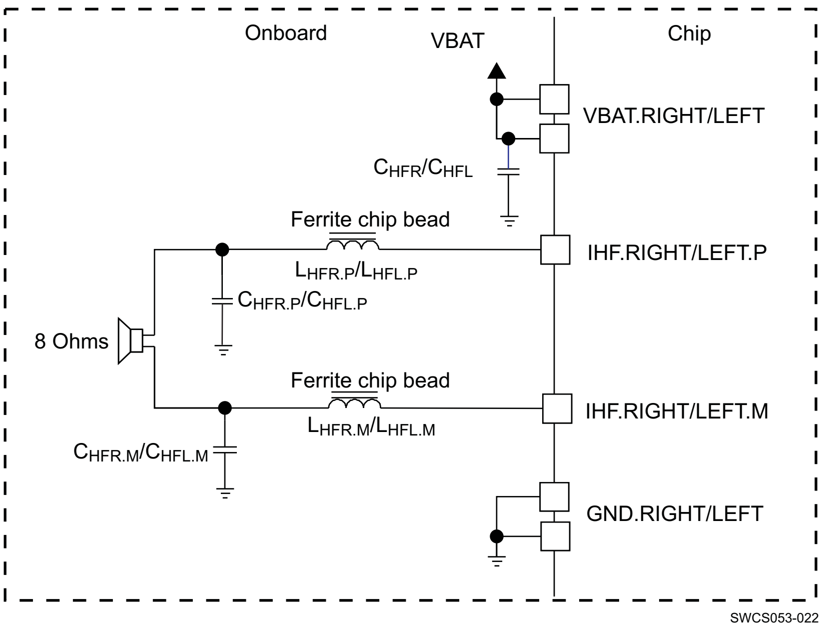


Figure 5-6. 8-Ω Stereo Hands-Free

NOTE

For the component values, see Table 12-1, *TPS65951 External Components*.

For ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies. Ferrite bead component examples are listed in the external components table, Table 12-1. Figure 5-7 shows the equivalent circuit for the ferrite bead.

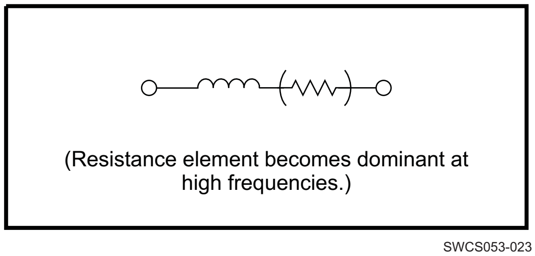


Figure 5-7. Ferrite Bead: Equivalent Circuit

5.1.3 Headset

Analog signal from the audio and/or voice interface is fed to two single-ended headset amplifiers.

There are two configurations:

- Stereo single-ended mode: Left and right headset amplifiers with different gains (–6 dB, 0 dB, 6 dB) provide the stereo signal on terminals HSOL and HSOR. A pseudo-ground is provided on terminal VMID to eliminate external capacitors.
- Stereo single-ended mode ac-coupled: Left and right headset amplifiers with different gains (–6 dB, 0 dB, 6 dB) provide the stereo signal on terminals HSOL and HSOR. The external capacitor is needed to eliminate the dc component of the signal.

5.1.3.1 Headset Output Characteristics

Figure 5-8 shows the headset amplifier. Table 5-3 summarizes the headset output characteristics.

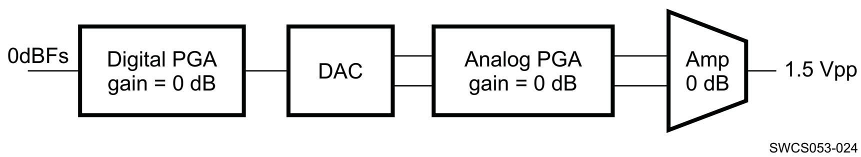
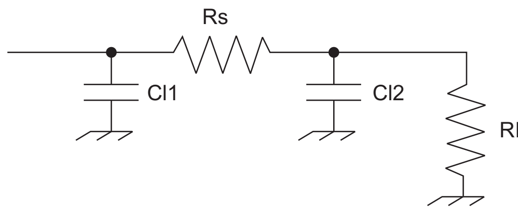


Figure 5-8. Headset Amplifier

Figure 5-9 shows the use case for an external high voltage driver connected to the headset output. The external high voltage driver for actuator is assumed to have analog input and connected to the left headset driver. To maintain headset driver stability, some guidelines related to the external load should be followed as shown below. An external serial resistor may be needed in case of large capacitive load.



External Load To Ensure Hs Driver Stability			
Cl1	Rs min	Cl2	Rl
<10p	0	<50p	>100K
	100	>50p <100p	
	300	>100p	
<10p	0	<50p	>1K <100K
	100	>50p <220p	
	300	>220p	
<10p	0	<200p	>14 <1K
	10	>200p <1n	
	33	>1n	

SWCS053-025

NOTE: For low impedance load, refer to Table 5-3.

Figure 5-9. Connection of External Actuator Driver to Headset Amplifier

Table 5-3. Headset Output Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load impedance		14	16	100k (1)	Ω
		0		100	pF
Gain range (2)	Audio path	–92		30	dB
	Voice path	–66		30	
Absolute gain error		–1		1	dB
Gain variation with frequency	F = 20 Hz to 20 kHz (Audio path, Fs = 48 kHz, 44.1 kHz)	–0.5		0.5	dB
Maximum output power	At 0.53 Vrms differential output voltage Load impedance = 16 Ω		17.56		mW
Peak-to-peak output voltage (0 dBFs)	Default gain (3)	1.34	1.5	1.68	V_{PP}
Single-Ended Mode AC-Coupled					
Total harmonic distortion Default gain (3) Load = 16 Ω	At 0 dBFs		–72	–67	dB
	At –6 dBFs		–74	–69	
	At –20 dBFs		–70	–65	
	At –60 dBFs		–30	–25	
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Default gain (3) Load = 16 Ω		–90	–85	dB
SNR (A-weighted over 20-kHz bandwidth)	At 0 dBFs	82	86		dB

(1) Refer to table in Figure 5-9 to ensure HS stability.
(2) Audio digital filter = –62 dB to 0 dB (1-dB step) and 0 dB to 12 dB (6-dB step)
Voice digital filter = –36 dB to 12 dB (1-dB step)
ARXPGA (volume control) = –24 dB to 12 dB (2-dB steps)
Output driver = –6 dB, 0 dB, 6 dB
(3) The default gain setting assumes the ARXPGA has 0 dB gain setting (volume control) and output driver at 0 dB gain setting.

Table 5-3. Headset Output Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output PSRR (for all gains)	20 Hz to 4 kHz		90		dB
	20 Hz to 20 kHz		70		
Crosstalk between right and left channels			–60		dB
Single-Ended Mode (Pseudo-Ground Provided on HSOVMID)					
Total harmonic distortion Default gain (3) Load = 16 Ω	At 0 dBFs		–70	–65	dB
	At –6 dBFs		–74	–69	
	At –20 dBFs		–70	–60	
	At –60 dBFs		–30	–25	
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Default gain (3) Load = 16 Ω		–90	–82	dB
Output PSRR (For all gains) versus VBAT (300mVpp)	20 Hz to 4 kHz		85		dB
	20 Hz to 20 kHz		65		

5.1.3.2 External Components and Application Schematics

Figure 5-10 shows the schematic for the headset 4-wire stereo jack without external FET.

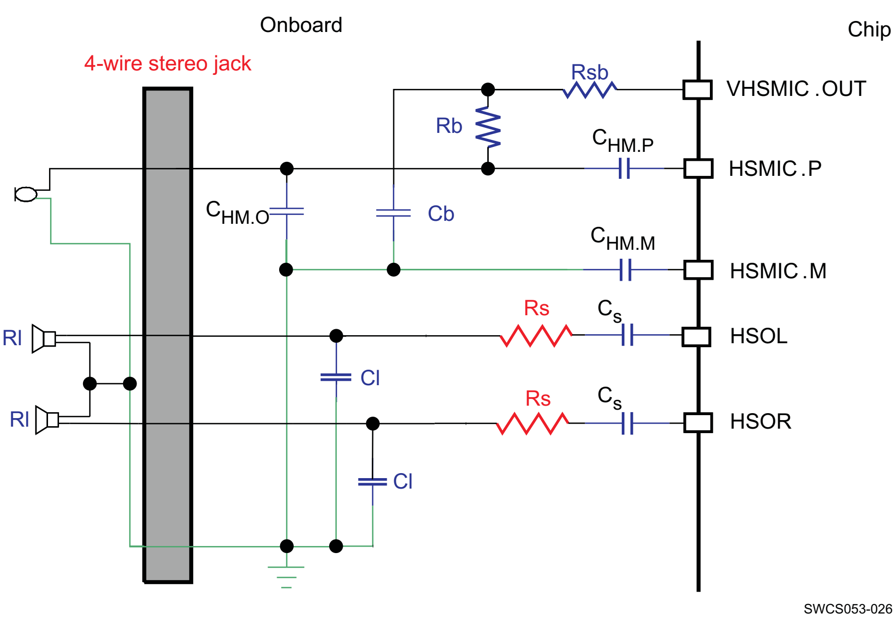


Figure 5-10. Headset 4-Wire Stereo Jack Without External FET

Table 5-4. Output Characteristics Headset 4-Wire Stereo Jack Without External FET

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Rsb	Cb < 200 pF		0			Ω
	Cb = 100 nF		300			
	Cb = 1 μF		500			
Rb+Rsb			2.2		2.7	kΩ
Cs The input capacitors and output resistors form a high-pass filter with the corner frequency = $1/(2\pi R_{out}/Cs)$			22	47		μF
Rs (serial resistance) needed to ensure HS amplifier stability	R_L	C_L				Ω
	16 Ω to 32 Ω	< 100 pF	0			
	16 Ω to 32 Ω	1 nF	4			
	16 Ω	2 nF	8			
	24 Ω		12			
	32 Ω		18			
	16 Ω	3 nF	12			
	24 Ω		20			
	32 Ω		24			
	16 Ω	4 nF	16			
	24 Ω		24			
	32 Ω		32			
	16 Ω	5 nF	20			
	24 Ω		28			
	32 Ω		36			

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

Table 5-5 shows the schematic for the headset 4-wire stereo jack with external FET.

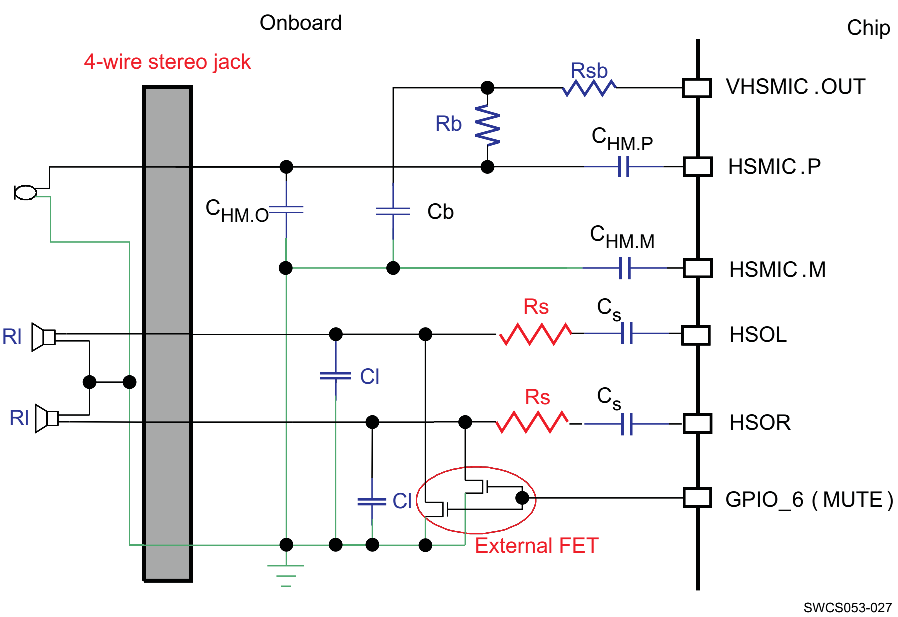


Figure 5-11. Headset 4-Wire Stereo Jack With External FET

Table 5-5. Output Characteristics Headset 4-Wire Stereo Jack With External FET

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Rsb	Cb < 200 pF		0			Ω
	Cb = 100 nF		300			
	Cb = 1 μF		500			
Rb+Rsb			2.2		2.7	kΩ
Cs The input capacitors and output resistors form a high-pass filter with the corner frequency = $1/(2\pi R_{out}/Cs)$			22	47		μF
	R_L	C_L				
Rs (serial resistance) needed to ensure HS amplifier stability and no distortion due to the parasitic diode of the external FET	16 Ω	< 2 nF	10			Ω
	24 Ω		15			
	32 Ω		20			
	16 Ω	3 nF	12			
	24 Ω		20			
	32 Ω		24			
	16 Ω	4 nF	16			
	24 Ω		24			
	32 Ω		32			
	16 Ω	5 nF	20			
	24 Ω		28			
	32 Ω		36			

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

Figure 5-12 shows the schematic for the headset 5-wire stereo jack.

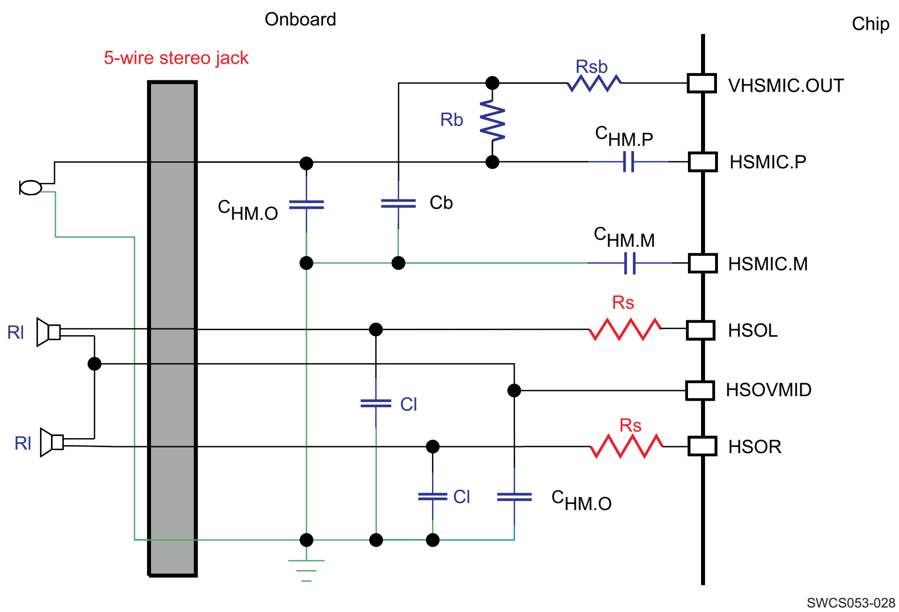


Figure 5-12. Headset 5-Wire Stereo Jack

Table 5-6. Output Characteristics Headset 5-Wire Stereo Jack

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Rsb	Cb < 200 pF		0			Ω
	Cb = 100 nF		300			
	Cb = 1 µF		500			
Rb+Rsb			2.2		2.7	kΩ
Rs (serial resistance) needed to ensure HS amplifier stability	**R_L**	**C_L**				Ω
	16 Ω to 32 Ω	< 100 pF	0			
	16 Ω to 32 Ω	1 nF	4			
	16 Ω	2 nF	8			
	24 Ω		12			
	32 Ω		18			
	16 Ω	3 nF	12			
	24 Ω		20			
	32 Ω		24			
	16 Ω	4 nF	16			
	24 Ω		24			
	32 Ω		32			
	16 Ω	5 nF	20			
	24 Ω		28			
	32 Ω		36			

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

Figure 5-13 shows the schematic for the headset 4-wire stereo jack optimized.

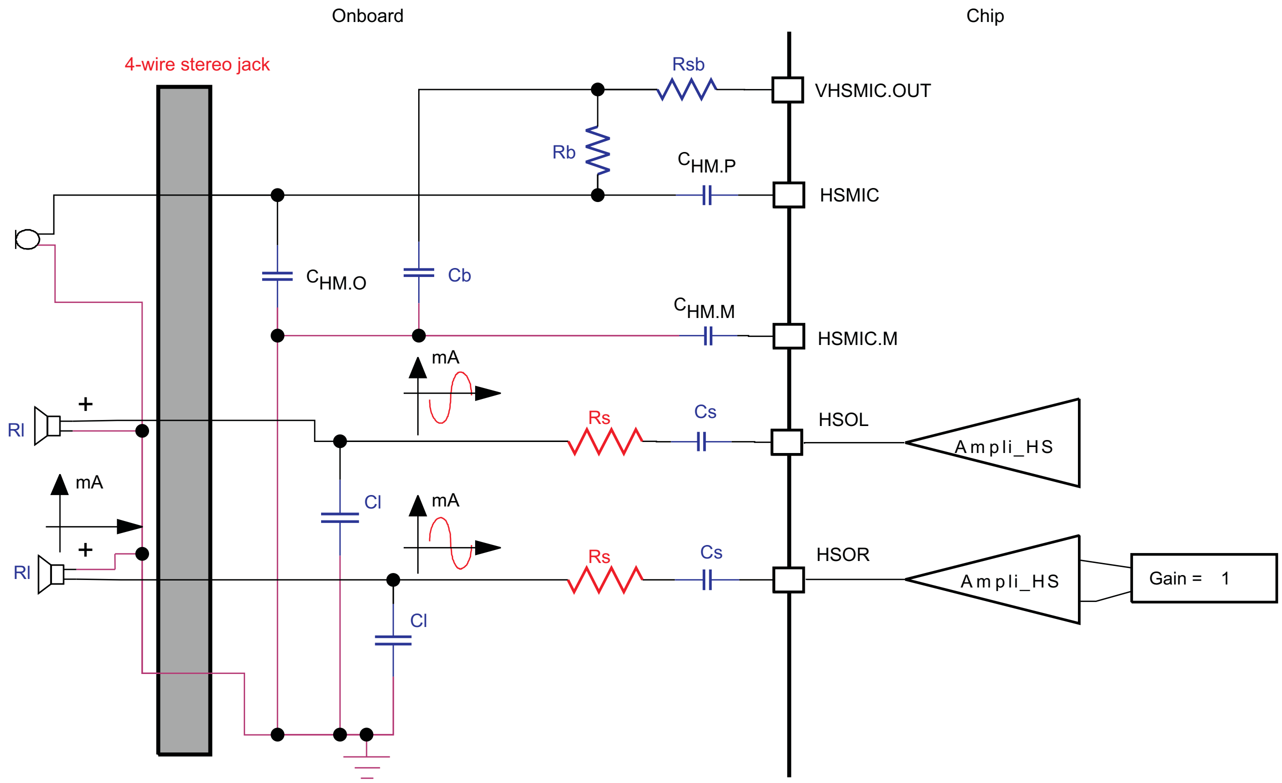


Figure 5-13. Headset 4-Wire Stereo Jack Optimized

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

5.1.4 Headset Pop-Noise Attenuation

Pop noise is due to the audio output amplifier being switched on. Although the speaker is ac-coupled through an external capacitor, the sharp rise time given by the activation of the amplifier causes a large spike to propagate to the speakers. Pop attenuation is achieved through a precharge and discharge of the external coupling capacitor.

The antipop system using an internal current generator controlling the ramp of charge or discharge is implemented for the headset output. The pop-noise effect can be dramatically reduced by an external FET controlled by a 1.8-V output signal (GPIO.6 pin).

Figure 5-14 shows the headset pop-noise diagram. Table 5-7 summarizes the headset pop-noise characteristics.

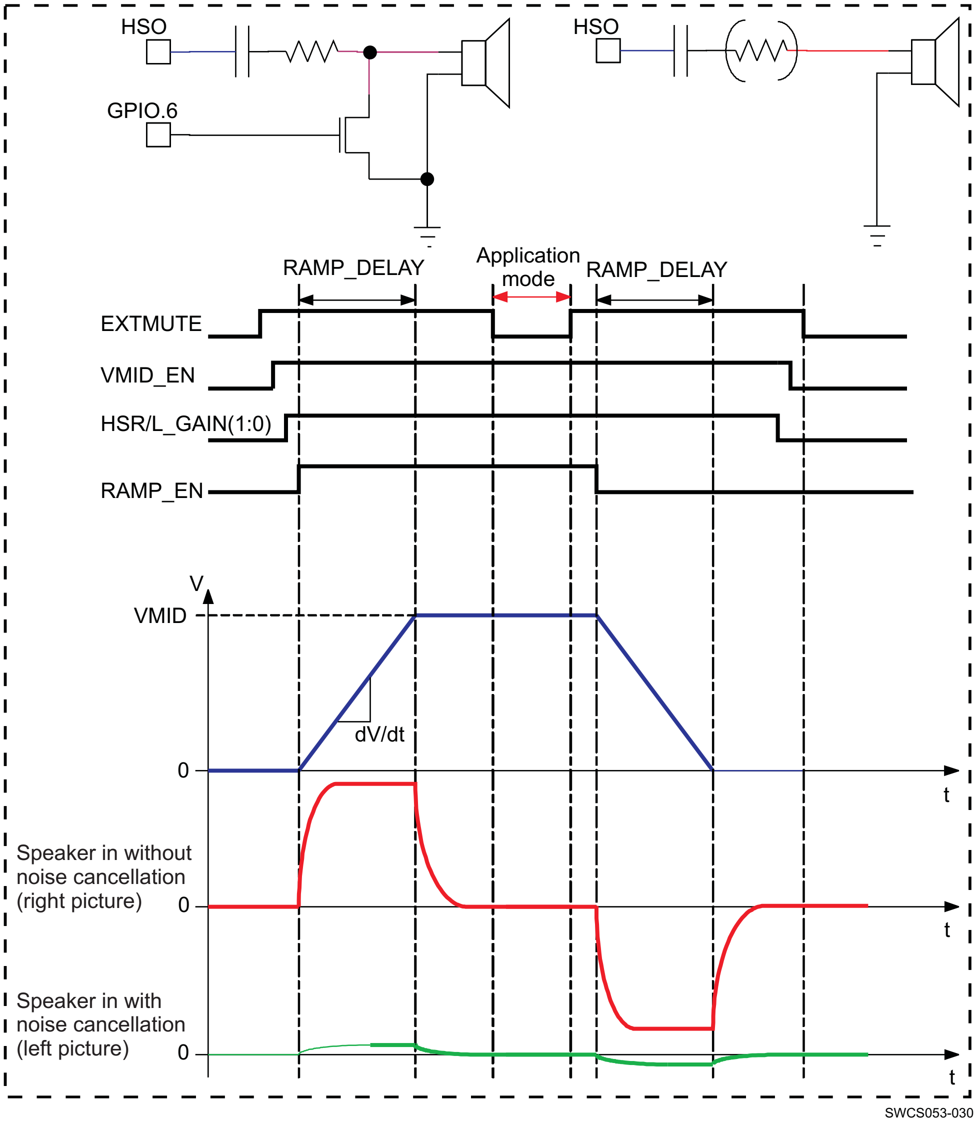


Figure 5-14. Headset Pop-Noise Cancellation Diagram

Table 5-7. Headset Pop-Noise Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
dv/dt	Ramp of charge or discharge			170	V/s
Pop-noise (A-weighted)	AC-coupling capacitor = 47 μF Serial resistor = 33 Ω External FET: Rdson = 0.12 Ω			1	mV

5.1.5 Predriver for External Class D Amplifier

These amplifiers provide a stereo signal on terminals PreD.LEFT and PreD.RIGHT to drive the external class D amplifier. These terminals are available if a stereo, single-ended, ac-coupled headset is used.

5.1.5.1 Predriver Output Characteristics

Table 5-8 summarizes the predriver output characteristics.

Table 5-8. Predriver Output Characteristics

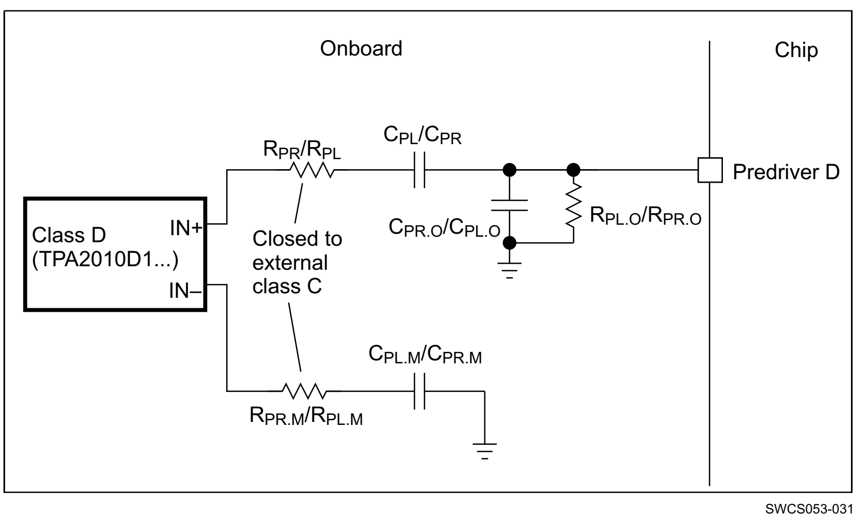
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load impedance		10		100	kΩ
		0		50	pF
Gain range (1)	Audio path	–92		30	dB
	Voice path	–66		30	
Absolute gain error		–1		1	dB
Peak-to-peak output voltage (0 dBFs)	Default gain (2)		1.5		V_{PP}
Total harmonic distortion Default gain (2) Load > 10 kΩ // 50 pF	At 0 dBFs		–80	–70	dB
	At –6 dBFs		–74	–69	
	At –20 dBFs		–70	–65	
	At –60 dBFs		–30	–25	
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Default gain (2) Load = 10 kΩ		–90	–85	dB
SNR (A-weighted over 20-kHz bandwidth) Default gain(2)	At 0 dBFs	80	88		dB
	At –60 dBFS		30		
Output PSRR (for all gains)	20 Hz to 4 kHz	80	90		dB
	20 Hz to 20 kHz	70	80		

(1) Audio digital filter = –62 dB to 0 dB (1-dB step) and 0 dB to 12 dB (6-dB step)
Voice digital filter = –36 dB to 12 dB (1-dB step)
ARXPGA (volume control) = –24 dB to 12 dB (2-dB steps)
Output driver = –6 dB, 0 dB, 6 dB

(2) The default gain setting assumes the ARXPGA has 0 dB gain setting (volume control) and output driver at 0 dB gain setting.

5.1.5.2 External Components and Application Schematics

Figure 5-15 shows a simplified schematic for the external class D predriver.



NOTE: Input resistor (R_{PR} or R_{PL}) sets the gain of the external Class D. For TPS2010D1, the gain is defined according to the following equation:
Gain (V/V) = $2 \times 150 \times 10^3/(R_{PR}$ or $R_{PL})$
R_{PR} or R_{PL} > 15 kΩ

Figure 5-15. Predriver for External Class D

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

5.1.6 Vibra H-Bridge

The digital signal from the pulse width modulated generator is fed to the Vibra H-bridge driver. The Vibra H-bridge is a differential driver and is used to drive Vibra motors. The differential output allows dual rotation directions.

5.1.6.1 Vibra H-Bridge Output Characteristics

Table 5-9 summarizes the Vibra H-bridge output characteristics.

Table 5-9. Vibra H-Bridge Output Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBAT voltage		2.8	3.6	4.8	V
Differential output swing (16-Ω load)	VBAT = 2.8 V	3.6			V_{PP}
	VBAT = 3.5 V	4.3			
Output resistance	Sum of the differential H-Bridge outputs (PMOS and NMOS output resistance)			5	Ω
Load capacitance				100	pF
Load resistance		8	16	60	Ω
Load inductance			30	300	μH
Total harmonic distortion	Input frequency: 20 Hz to 10 kHz			10%	

5.1.6.2 External Components and Application Schematics

Figure 5-16 shows a simplified Vibra H-bridge schematic.

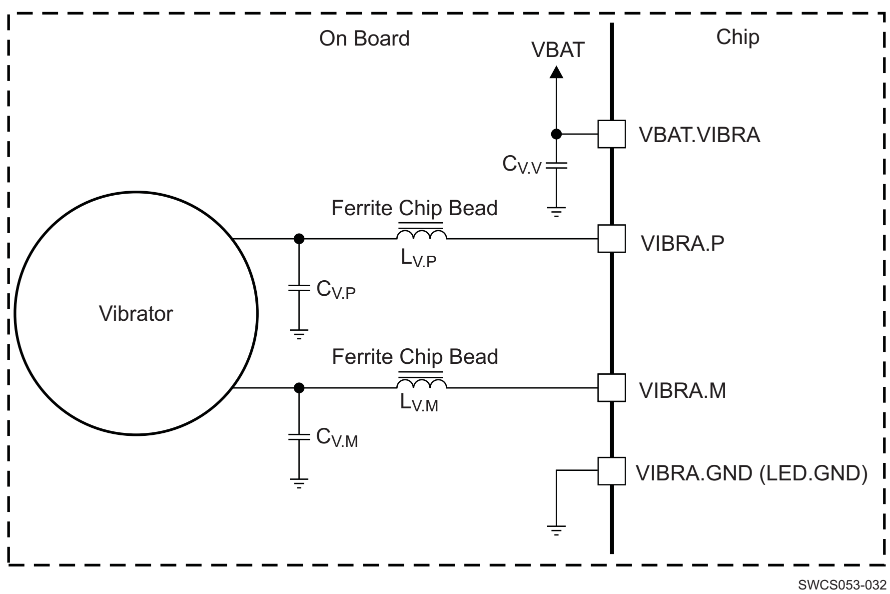


Figure 5-16. Vibra H-Bridge

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

Example of ferrite: BLM 18BD221SN1.

5.1.7 Digital Audio Filter Module

Figure 5-17 shows the digital audio filter downlink full path characteristics for the audio interface.

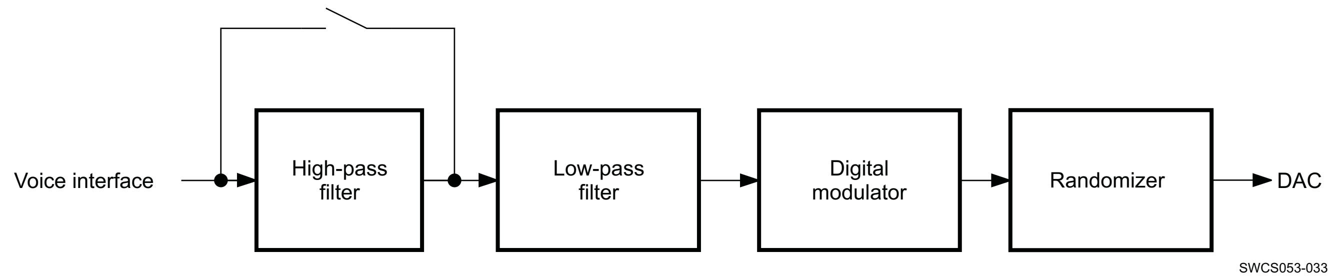


Figure 5-17. Digital Audio Filter Downlink Path Characteristics

The high-pass filter can be bypassed. It is controlled by register MISC_SET_2, address 0x49, ARX_HPF_BYP bit.

Table 5-10 shows the audio filter frequency response relative to reference gain at 1 kHz.

Table 5-10. Digital Audio Filter RX Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Passband			0.42		F_S
Passband ripple	0 to 0.42F_S (1)	–0.25	0.1	0.25	dB
Stopband			0.6		F_S
Stopband attenuation	F = 0.6F_S (1) to 0.8F_S (1)	60	75		dB
Group delay			15.8/F_S (1)		µs
Linear phase		–1.4		1.4	°

(1) F_S is the sampling frequency (8, 11.025, 12, 16, 22.05, 24, 32, 44.1, or 48 kHz).

5.1.8 Digital Voice Filter Module

Figure 5-18 shows the digital voice filter downlink full path characteristics for the voice interface.

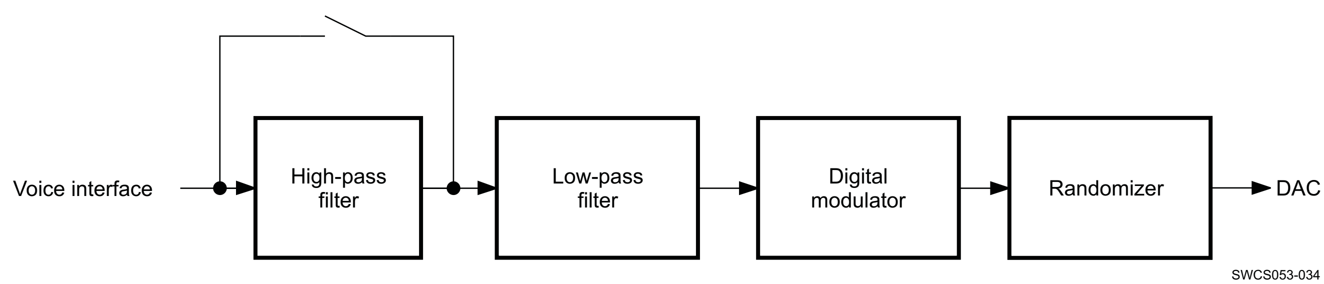


Figure 5-18. Digital Voice Filter Downlink Path Characteristics

The global high-pass filter or only the 3rd order high-pass filter can be bypassed (when 3rd order HPF is skipped, 1st order is still active). It is controlled by register MISC_SET_2, address 0x49, VRX_3RD_HPF_BYP bit for the 3rd order high-pass filter, and the VRX_HPF_BYP bit for the global high-pass filter.

5.1.8.1 Voice Downlink Filter (with Sampling Frequency at 8 kHz)

Figure 5-19 and Table 5-11 show the voice filter frequency response relative to the reference gain at 1 kHz with F_S = 8 kHz.

Table 5-11. Digital Voice Filter RX Electrical Characteristics with F_S = 8 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response relative to reference gain at 1 kHz	100 Hz			–20	dB
	200 Hz	–8		–0.5	
	300 Hz to 3300 Hz	–0.5	0	0.5	
	3400 Hz	–1.5	0	0.1	
	4000 Hz			–17	
	4600 Hz			–40	
	> 6000 Hz			–45	
Pole when 3rd order high-pass filter is disabled (1st order HPF)			2.5		Hz
Group delay			0.5		ms

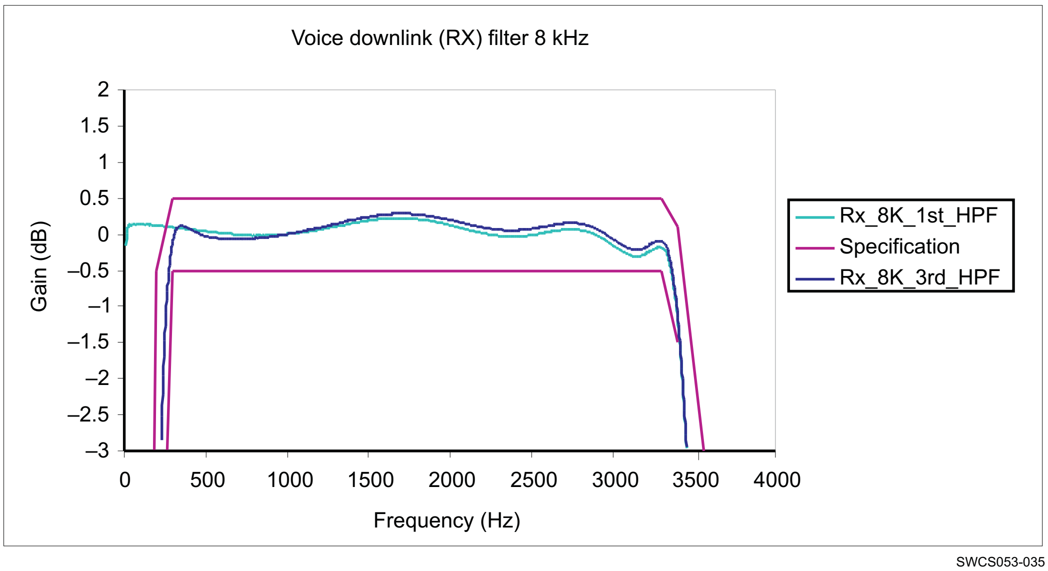


Figure 5-19. Voice Downlink Frequency Response F_S = 8 kHz

5.1.8.2 Voice Downlink Filter (with Sampling Frequency at 16 kHz)

Table 5-12 and Figure 5-20 show the voice filter frequency response relative to the reference gain at 1 kHz with F_S = 16 kHz.

Table 5-12. Digital Voice Filter RX Electrical Characteristics with F_S = 16 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response relative to reference gain at 1 kHz (1st order HPF)	300 Hz to 6600 Hz	–0.5	0	0.5	dB
	6800 Hz	–1.5	0	0.1	
	8000 Hz			–17	
	9200 Hz			–40	
	> 12000 Hz			–45	
Pole when 3rd order high-pass filter is disabled (1st order HPF)			5		Hz

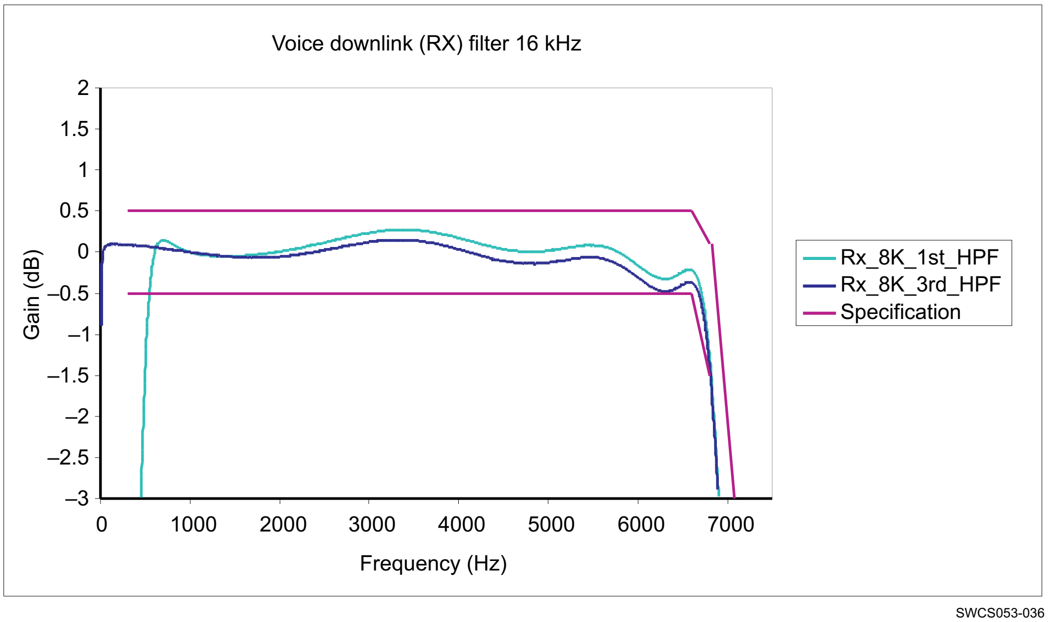


Figure 5-20. Voice Downlink Frequency Response F_S = 16 kHz

5.1.9 Boost Stage

The boost effect is used to add emphasis to low frequencies. It is used to compensate high-pass filter created by the CR (capacitor resistor) filter of the headset (in ac-coupling configuration).

There are four modes thus three available effects with slightly different frequency responses. The fourth setting disables the boost effect.

The following four modes are described with their equalization profile:

- Flat equalization: The boost effect is in bypass mode.
- Boost (effect) 1 / 2 / 3 modes are defined as below.

Table 5-13 and Table 5-14 include the typical values according the frequency response versus input frequency and Fs frequency.

Table 5-13. Boost Electrical Characteristics vs F_S Frequency ($F_S \leq 22.05$ kHz)

Frequency (Hz)	F_S = 8 kHz			F_S = 11.025 kHz			F_S = 12 kHz			F_S = 16 kHz			F_S = 22.05 kHz			Unit
	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	
10	4.51	5.13	5.62	5.10	5.51	5.80	5.22	5.58	5.83	5.54	5.77	5.92	5.76	5.89	5.97	dB
12	4.08	4.83	5.46	4.80	5.32	5.71	4.95	5.41	5.76	5.36	5.66	5.87	5.65	5.83	5.94	
15.2	3.43	4.32	5.18	4.28	4.97	5.54	4.47	5.11	5.61	5.03	5.47	5.79	5.45	5.71	5.90	
18.2	2.91	3.86	4.89	3.82	4.63	5.36	4.04	4.80	5.45	4.71	5.26	5.69	5.24	5.59	5.84	
20.5	2.56	3.53	4.65	3.49	4.37	5.21	3.72	4.56	5.32	4.45	5.09	5.60	5.06	5.49	5.79	
29.4	1.62	2.49	3.78	2.45	3.42	4.57	2.68	3.74	4.73	3.51	4.39	5.24	4.35	5.02	5.59	
39.7	1.05	1.71	2.93	1.67	2.55	3.84	1.88	2.80	4.06	2.66	3.63	4.72	3.67	4.45	5.27	
50.4	0.71	1.20	2.26	1.17	1.91	3.17	1.33	2.13	3.41	2.01	2.95	4.19	2.89	3.85	4.88	
60.3	0.51	0.92	1.79	0.89	1.49	2.65	1.00	1.68	2.89	1.57	2.43	3.72	2.39	3.35	4.52	
76.7	0.32	0.61	1.26	0.59	1.05	1.99	0.69	1.18	2.22	1.11	1.79	3.04	1.76	2.66	3.94	
97.5	0.20	0.39	0.87	0.38	0.70	1.43	0.44	0.79	1.62	0.75	1.27	2.36	1.24	2.00	3.28	
131.5	0.12	0.21	0.50	0.20	0.39	0.88	0.25	0.47	1.02	0.42	0.78	1.59	0.75	1.30	2.41	
157	0.08	0.15	0.36	0.15	0.28	0.65	0.17	0.33	0.75	0.31	0.57	1.22	0.55	0.99	1.93	
200	0.05	0.09	0.22	0.09	0.17	0.41	0.11	0.21	0.49	0.19	0.37	0.82	0.36	0.66	1.38	
240	0.03	0.06	0.15	0.06	0.12	0.29	0.07	0.14	0.35	0.14	0.26	0.60	0.25	0.48	1.04	
304	0.02	0.04	0.09	0.04	0.07	0.18	0.04	0.09	0.22	0.08	0.16	0.38	0.16	0.30	0.70	
463	0.00	0.01	0.03	0.01	0.03	0.07	0.02	0.04	0.09	0.03	0.07	0.17	0.07	0.13	0.32	
704	0.00	0.00	0.01	0.00	0.01	0.03	0.01	0.01	0.03	0.01	0.03	0.07	0.03	0.06	0.14	
1008	0.00	0.00	0.00	0.00	0.00	0.01	0.00	0.00	0.01	0.00	0.01	0.03	0.01	0.02	0.06	
1444	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.01	0.02	
2070	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.01	
3770	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	

Table 5-14. Boost Electrical Characteristics vs F_S Frequency ($F_S \geq 24$ kHz)

Frequency (Hz)	F_S = 24 kHz			F_S = 32 kHz			F_S = 44.1 kHz			F_S = 48 kHz			F_S = 96 kHz			Unit
	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	
10	5.79	5.90	5.97	5.89	5.89	5.99	5.95	5.98	6.04	5.96	5.99	6.01	5.71	5.83	5.90	dB
12	5.70	5.85	5.95	5.84	5.84	5.98	5.92	5.97	6.03	5.94	5.98	6.00	5.54	5.68	5.81	
15.2	5.53	5.76	5.91	5.73	5.73	5.96	5.87	5.94	6.02	5.89	5.95	5.99	5.40	5.57	5.73	
18.2	5.35	5.65	5.87	5.62	5.62	5.93	5.80	5.90	6.00	5.83	5.93	5.98	5.28	5.48	5.68	
20.5	5.19	5.56	5.83	5.52	5.52	5.91	5.74	5.87	5.99	5.78	5.90	5.97	5.19	5.42	5.64	
29.4	4.55	5.18	5.64	5.10	5.07	5.79	5.51	5.75	5.94	5.57	5.79	5.92	4.87	5.18	5.48	
39.7	3.81	4.62	5.37	4.52	4.52	5.64	5.12	5.53	5.85	5.26	5.59	5.84	4.47	4.91	5.30	
50.4	3.14	4.06	5.02	3.94	3.95	5.43	4.69	5.27	5.72	4.88	5.37	5.73	4.08	4.63	5.11	
60.3	2.62	3.51	4.69	3.46	3.54	5.21	4.30	5.00	5.59	4.49	5.13	5.62	3.72	4.37	4.95	
76.7	1.97	2.90	4.15	2.76	2.76	4.78	3.68	4.52	5.34	3.91	4.70	5.40	3.18	3.92	4.67	
97.5	1.41	2.22	3.51	2.10	2.09	4.27	2.99	3.94	4.99	3.24	4.15	5.07	2.59	3.41	4.33	
131.5	0.88	1.49	2.65	1.40	1.40	3.49	2.15	3.10	4.35	2.38	3.35	4.51	1.86	2.69	3.75	
157	0.65	1.13	2.15	1.04	1.04	2.96	1.70	2.58	3.90	1.90	2.82	4.08	1.47	2.24	3.35	
200	0.41	0.76	1.55	0.70	0.70	2.28	1.19	1.93	3.23	1.35	2.15	3.44	1.03	1.68	2.77	
240	0.30	0.55	1.18	0.50	0.50	1.81	0.89	1.51	2.71	1.02	1.70	2.92	0.77	1.31	2.32	
304	0.18	0.35	0.80	0.33	0.32	1.27	0.58	1.04	2.05	0.68	1.19	2.24	0.51	0.90	1.75	
463	0.08	0.16	0.37	0.14	0.14	0.64	0.27	0.50	1.12	0.31	0.58	1.25	0.23	0.43	0.95	
704	0.03	0.06	0.16	0.06	0.06	0.29	0.12	0.23	0.56	0.14	0.27	0.62	0.10	0.20	0.46	
1008	0.01	0.03	0.07	0.03	0.02	0.14	0.06	0.11	0.30	0.06	0.13	0.31	0.05	0.10	0.23	
1444	0.00	0.01	0.03	0.01	0.01	0.06	0.03	0.05	0.16	0.03	0.06	0.15	0.02	0.05	0.11	
2070	0.00	0.00	0.01	0.00	0.00	0.02	0.01	0.02	0.09	0.01	0.03	0.07	0.01	0.02	0.05	
3770	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.04	0.00	0.00	0.01	0.00	0.00	0.01	

5.2 Audio/Voice Uplink (TX) Module

The voice uplink path includes two input amplification stages dedicated to nine analog input terminals:

- MIC.MAIN.P, MIC.MAIN.M (differential main handset input)
- MIC.SUB.P, MIC.SUB.M (differential sub handset input)
- HSMIC.P, HSMIC.M (differential headset input), HSMIC.DC (headset accessory detection)
- AUXL (common terminal: single-ended auxiliary/FM radio left channel input)
- AUXR (common terminal: single-ended auxiliary/FM radio right channel input)

For all cases, only two analog input amplifiers can be used because two ADC are available.

The voice uplink path also includes two PDM interfaces for digital microphone. Two stereo digital microphone interfaces are available.

The FM radio left and right channels can be connected to any of the audio output stages (for example, earpiece, headset speakers, etc.) through a connection matrix.

5.2.1 MIC Bias Module

Three bias generators provide an external voltage of 2.2 V to bias the analog microphones (MICBIAS1.OUT, MICBIAS2.OUT, and VHSMIC.OUT terminals). The typical current is between 300 and 500 µA, depending on the microphone impedance.

Bias generators can provide an external voltage of 1.8 V to bias digital microphone, DIG.MIC.0. The typical output current is 5 mA for each digital bias microphone.

Figure 5-21 shows the multiplexing for the analog and digital microphone.

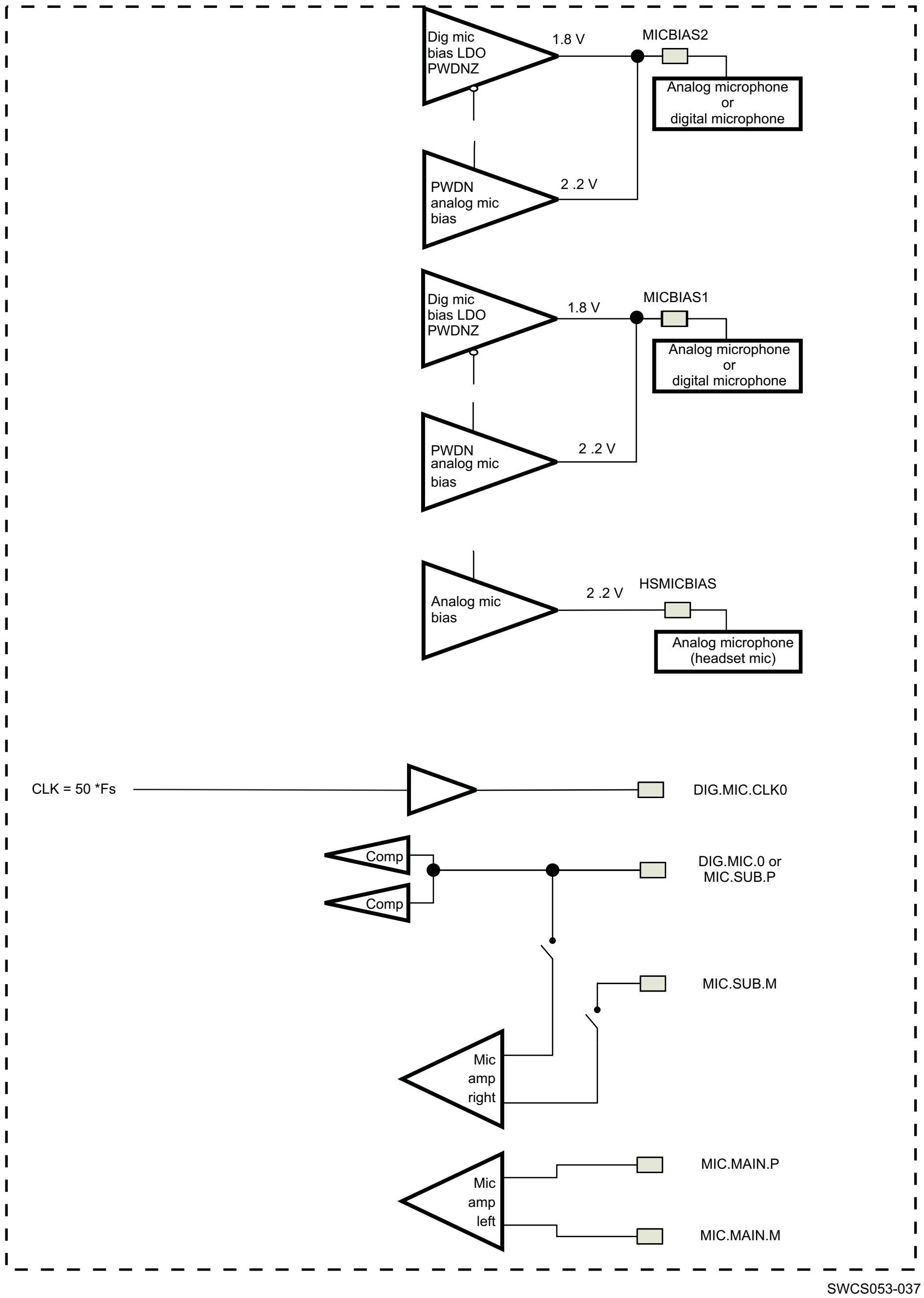


Figure 5-21. Analog and Digital Microphone Muxing

5.2.1.1 Analog MIC Bias Module Characteristics

Table 5-15. Analog Microphone Bias Module Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Bias voltage		2.15	2.2	2.25	V
Load current				1.2	mA
Output noise	P-weighted 20 Hz to 6.6 kHz			1.8	μV_{RMS}

Table 5-15. Analog Microphone Bias Module Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
External capacitor(1)		0		200	pF
Internal resistance(2)		50	60	70	kΩ
Quiescent current			350	390	μA
Start-up time				10	μs
PSRR from VBAT (300 mVpp)	From 20 Hz to 6.6 kHz	100			dB

(1) If the external capacitor is higher than 200 pF, then the analog microphone bias becomes unstable. To stabilize it, a serial resistor needs to be added.
(2) This resistance is an internal resistance of MIC Bias connected to the ground (in the feedback loop). When LDO is disabled, the DC impedance is higher than 1 MΩ.

Table 5-16. Analog Microphone Bias Module Characteristics, Bias Resistor

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{SB}	C_B < 200 pF	0			Ω
	C_B = 50 nF	100			
	C_B = 220 nF	200			
	C_B = 1 μF	500			
$R_B + R_{SB}$			2.2 to 2.7		kΩ

Figure 5-22 and Figure 5-23 show the external components and application schematics for the analog microphone.

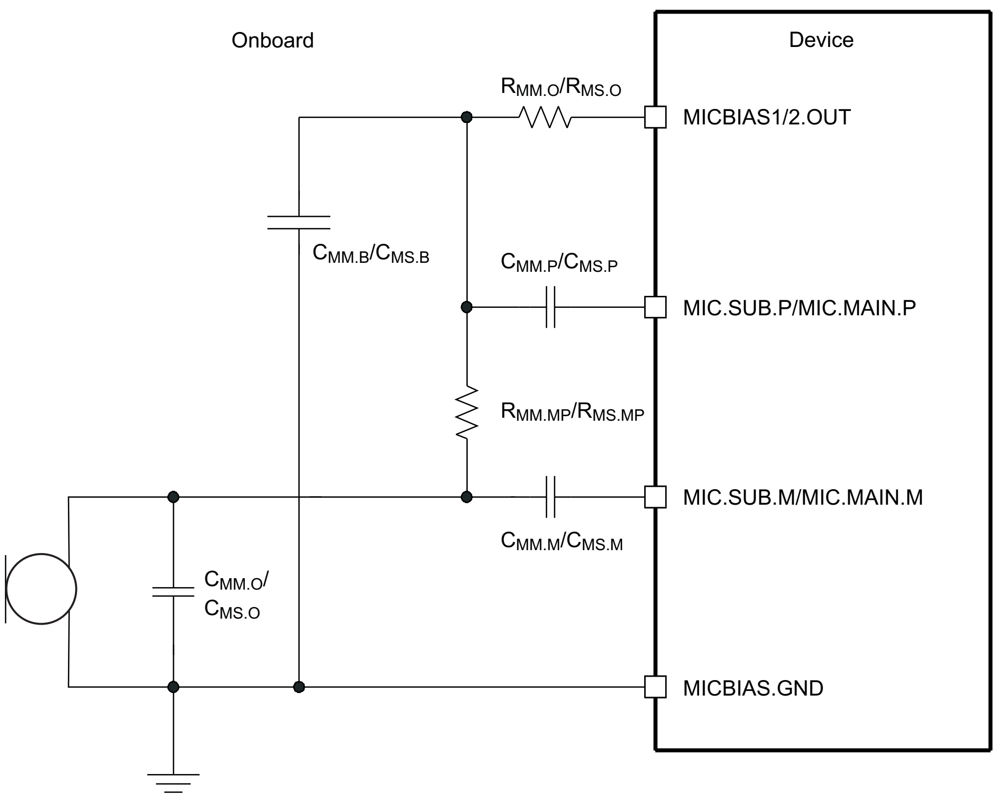


Figure 5-22. Analog Microphone Pseudodifferential

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

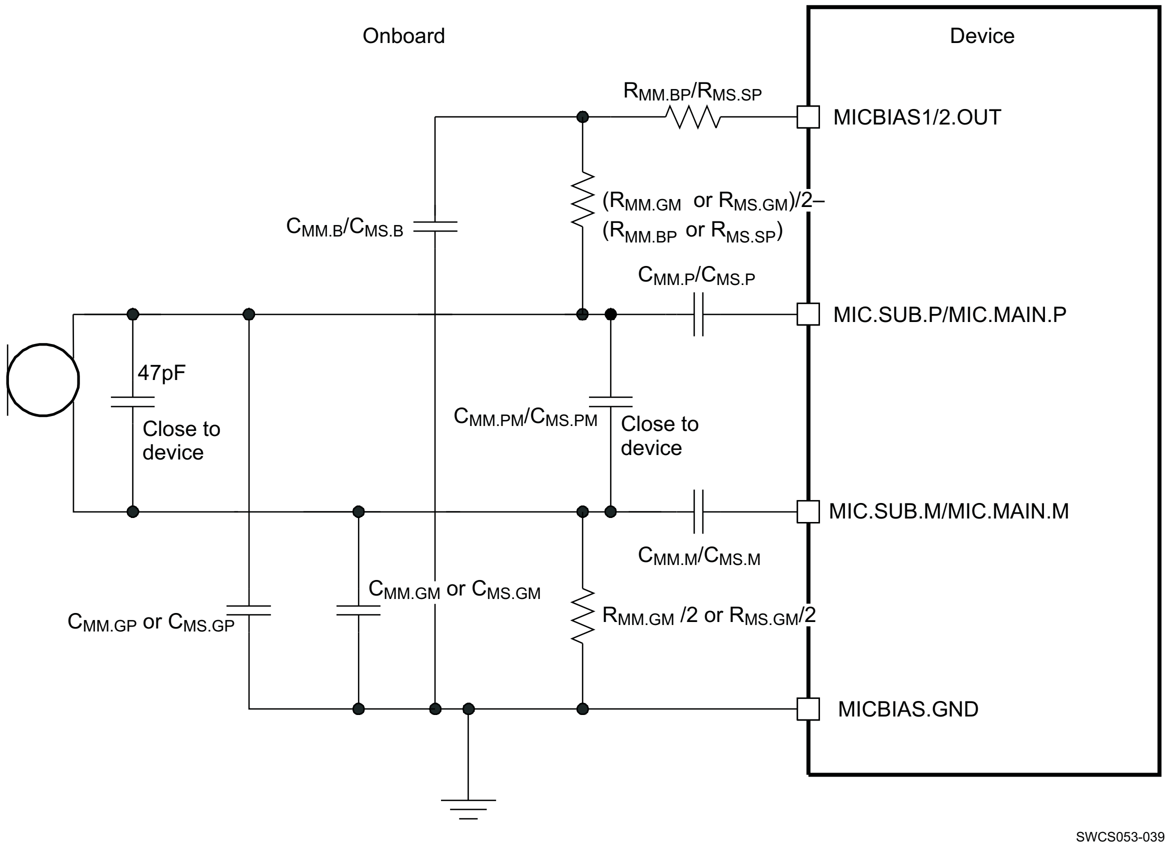


Figure 5-23. Analog Microphone Differential

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

NOTE

To improve the rejection, it is highly recommended to ensure a MICBIAS.GND as clean as possible. This ground must be shared with AGND of TPS65951 and must not share with AVSS4 which is the ground used by RX Class AB output stages.

In differential mode, adding a low-pass filter (made by R_{SB} and C_B) is highly recommended if coupling between RX output stages and the microphone is too high (and not enough attenuation by the echo cancellation algorithm). The coupling can come from:

- The internal TPS65951 coupling between MICBIAS1/2.OUT voltage and RX output stages.
- Coupling noise between MICBIAS.GND and AVSS4.

In pseudodifferential mode, the dynamic resistance of the microphone improves the rejection versus MICBIAS1/2.OUT:

$PSRR = 20 \times \log((R_B + R_{Dyn_mic})/R_B)$.

5.2.1.2 Digital MIC Bias Module Characteristics

Table 5-17. Digital Microphone Bias Module Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Bias voltage		1.75	1.8	1.85	V
Load current				10	mA
PSRR (from VBAT)	20 Hz to 6.6 kHz	60			dB
External capacitor		0.3	1	3.3	µF
ESR for capacitor	At 100 kHz	0.02		0.6	Ω
Start-up time				70	µs
Quiescent current				165	µA

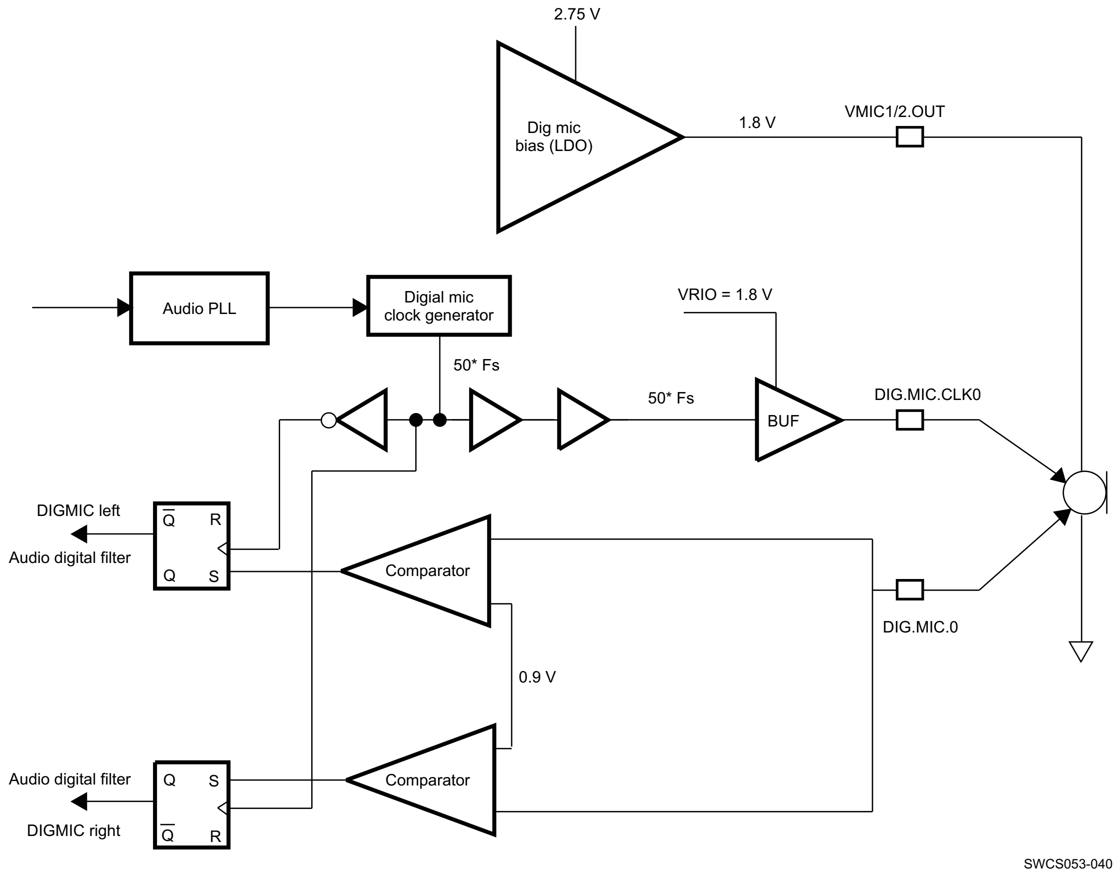


Figure 5-24. Digital Microphone Block Diagram

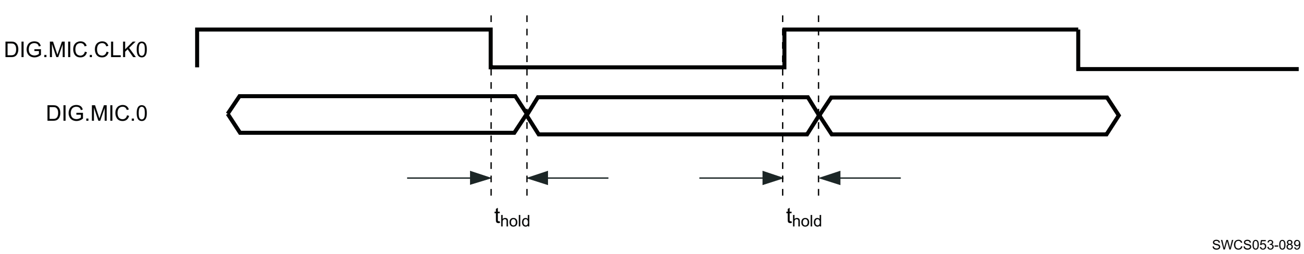


Figure 5-25. Digital Microphone Timing Diagram

Table 5-18. Digital Microphone Module Characteristics (2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator high threshold			0.5 × VDD_IO	0.7 × VDD_IO	
Comparator low threshold		0.3 × VDD_IO	0.5 × VDD_IO		
Start-up time				2	ms
DIG.MIC.0 (t_{HOLD}) from DIG.MIC.CLK0 edge		4			ns

5.2.1.3 Silicon MIC Module Characteristics

Based on silicon MEMS (micro-electrical-mechanical system) technology, the new microphone achieves the same acoustic and electrical properties as conventional microphones, but is more rugged and exhibits higher heat resistance. These properties offer designers of a wide range of products greater flexibility and new opportunities to integrate microphones.

The silicon microphone is the integration of mechanical elements and electronics on a common silicon substrate through microfabrication technology.

Moreover, the CMOS MEMS microphone is more like an analog IC than an ECM (classical microphone, Electret Condenser Microphone). It is powered as an IC with a direct connection to the power supply. The on-chip isolation between the power input and the rest of the system adds PSR to the component, making the CMOS MEMS microphone inherently more immune to power supply noise than an ECM and eliminating the need for additional filtering circuitry to keep the power supply line clean.

Table 5-19. Silicon Microphone Module Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Bias voltage			2.2		V
Load current				1	mA
Output noise	P-weighted 20 Hz to 6.6 kHz			1.8	μV_{RMS}

Figure 5-26 shows a schematic for the silicon microphone.

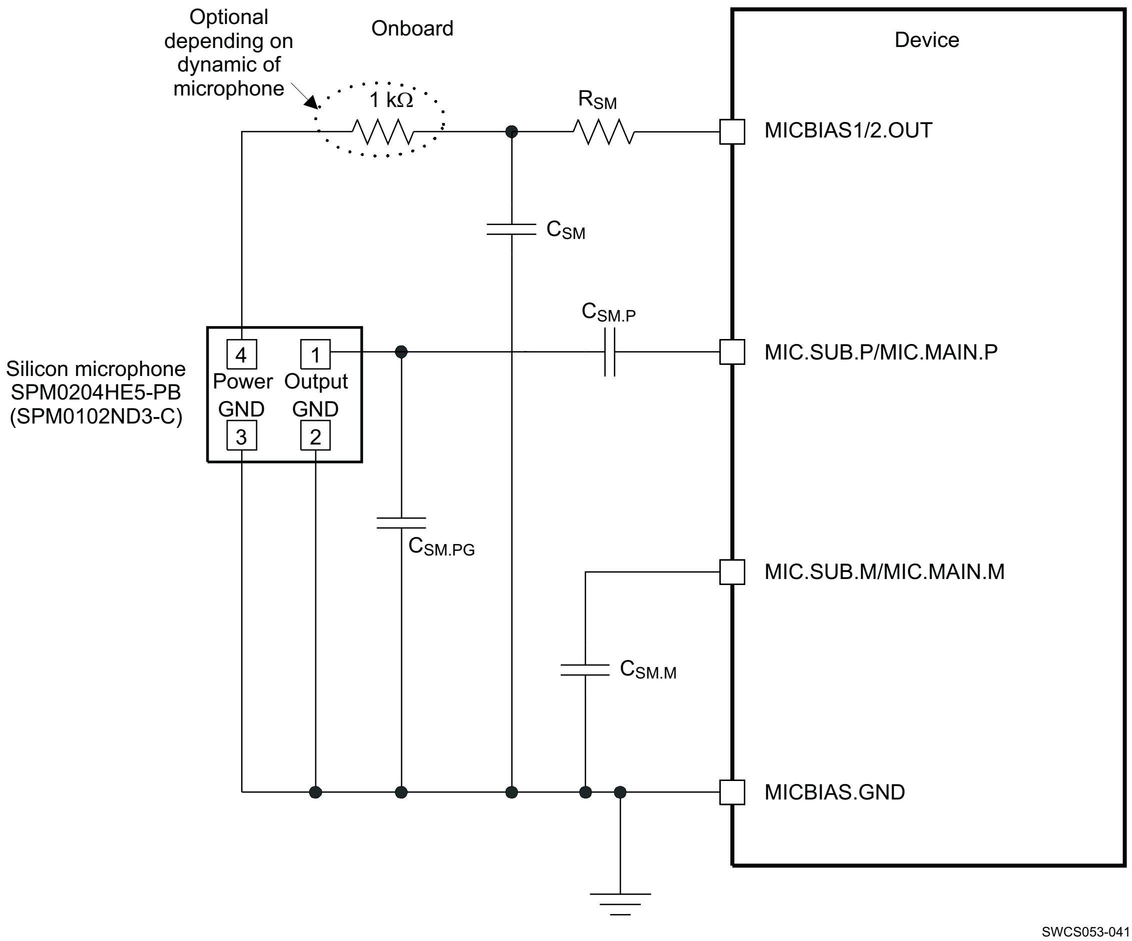


Figure 5-26. Silicon Microphone

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

5.2.2 *Stereo Differential Input*

The stereo differential inputs (MIC.MAIN.P, MIC.MAIN.M and MIC.SUB.P, MIC.SUB.M terminals) can be amplified by the microphone amplification stages. The amplification stage outputs are connected to the two ADC inputs.

5.2.3 *Headset Differential Input*

The headset differential inputs (HSMICP and HSMICM terminals) can be amplified by the microphone amplification stage. The amplification stage outputs are connected to the ADC input.

5.2.4 FM Radio/Auxiliary Stereo Input

The auxiliary inputs AUXL/FML and AUXR/FMR can be used as FM radio left and right stereo inputs. In that case (because both input amplifiers are busy), the other input terminals are discarded and set to a high impedance state. Both microphone amplification stages amplify the FM radio stereo signal. Both amplification stage outputs are connected to the ADC input. The FM radio left and right channels inputs can also be output through an audio output stage (mono output stage in case of mono input FM radio, stereo output stage in case of stereo input FM radio).

5.2.4.1 External Components

Figure 5-27 shows the external components on the auxiliary stereo input.

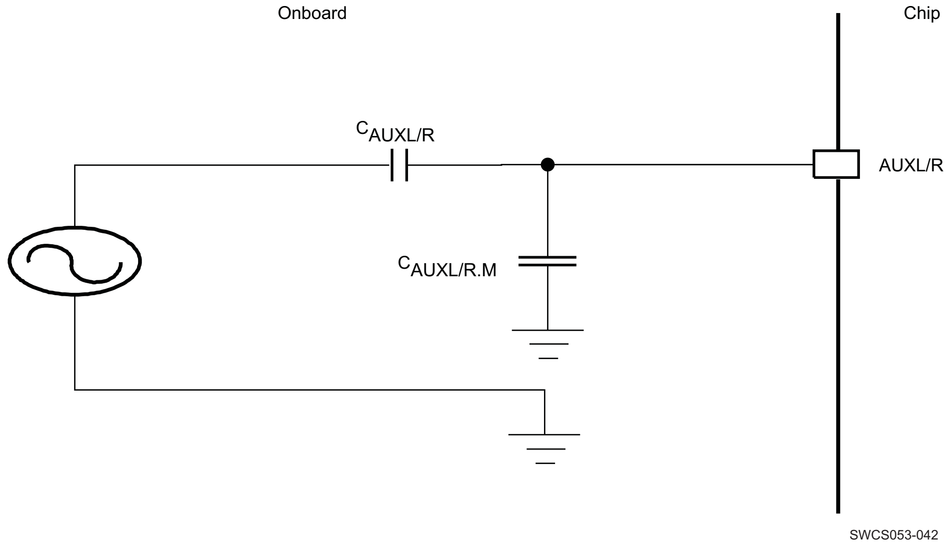


Figure 5-27. Audio Auxiliary Input

NOTE

For other values regarding the components, see Table 12-1, *TPS65951 External Components*.

5.2.5 Pulse Density Modulated (PDM) Interface for Digital Microphone

The PDM interface is used as digital microphone inputs: each microphone is directly connected to the TX filter decimator to extract the audio samples at desired accuracy and sample rate. Each digital microphone is stereo (2 paths). The digital microphone interface is DIG.MIC.CLK (clock input to the microphone) and DIG.MIC (PDM data output from the microphone). The appropriate frequency of DIG.MIC.CLK is generated by the audio PLL, and the ratio between DIG.MIC.CLK and sample rate is equal to 50 (see Figure 5-28). The PDM interface is available only when f_S = 48 kHz.

The data signal output is a 3-state output from the microphone. When a falling edge DIG.MIC.CLK is detected, the DIG.MIC is actively driven. When a rising DIG.MIC.CLK is detected, the DIG.MIC is high impedance. The latter DIG.MIC.CLK half-cycle is reserved for stereo operation (the second microphone receives DIG.MIC.CLK inverted).

The Σ-Δ converter inside the digital microphone produces pulse density modulated (PDM).

Digital microphone characteristics:

- PDM clock rate 2.4 MHz
- 4th order Σ-Δ converter inside the microphone component
- 0 db PDM inputs involves 0dBFs data output (with default gain setting: 0 db)

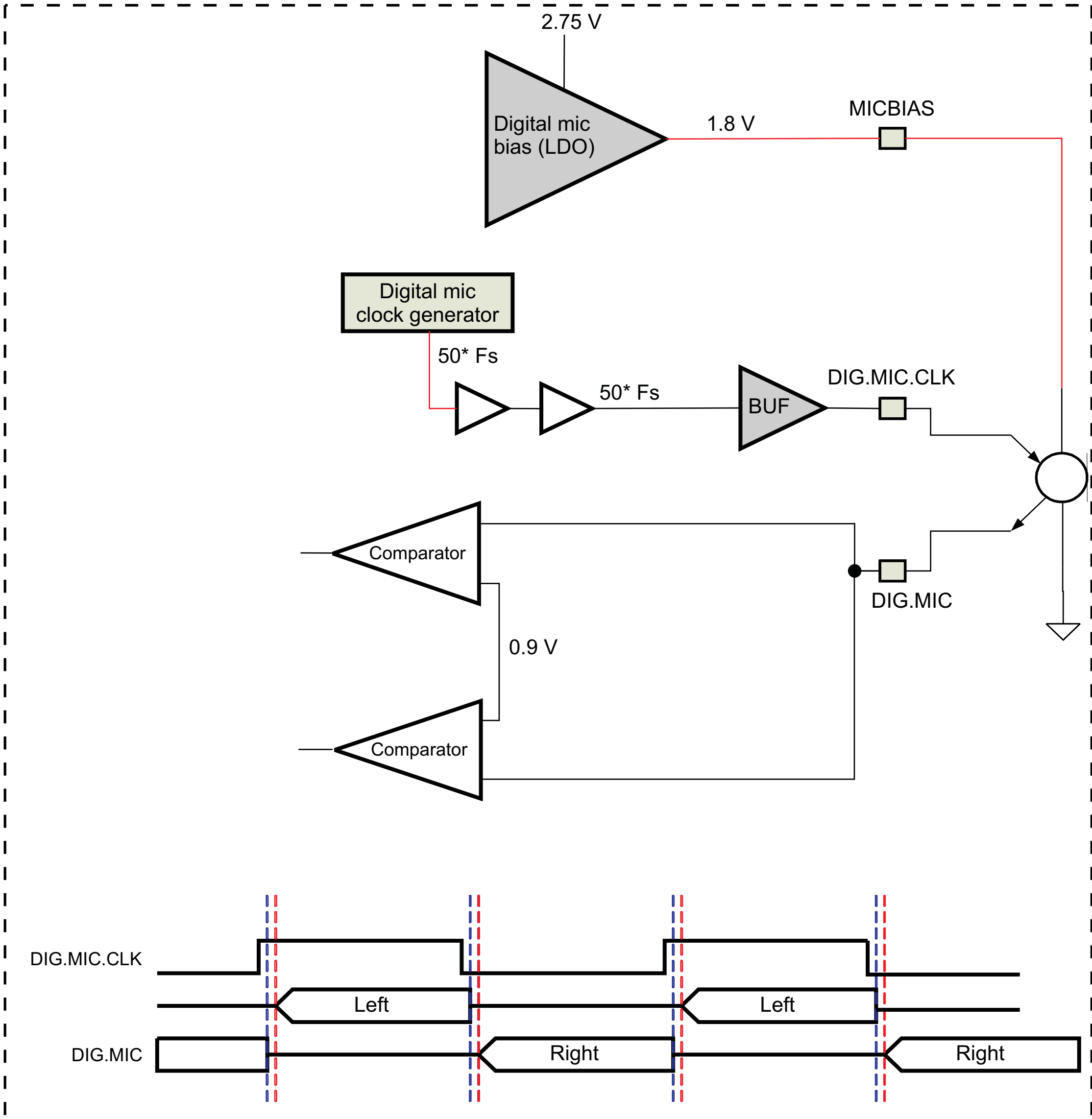


Figure 5-28. Example of Circuitry

5.2.6 Uplink Characteristics

Figure 5-29 shows the uplink amplifier. Table 5-20 summarizes the uplink characteristics.

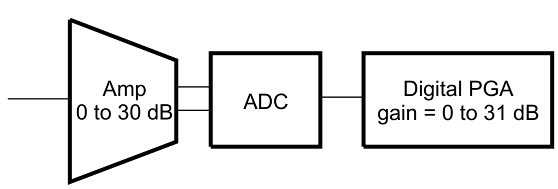


Figure 5-29. Uplink Amplifier

Table 5-20. Uplink Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speech delay	Voice path		0.5		ms
Gain range(1)		0		61	dB
Absolute gain	0 dBFs at 1.02 kHz	–1		1	dB
Peak-to-peak differential input voltage (0 dBFs)	For differential input 0 dB gain setting			1.5	V_{PP}
Peak-to-peak single-ended input voltage (0 dBFs)	For single-ended input 0 dB gain setting			1.5	V_{PP}
Total harmonic distortion (sine wave at 1.02 kHz)	At –1 dBFs		–80	–75	dB
	At –6 dBFs		–74	–69	
	At –10 dBFs		–70	–65	
	At –20 dBFs		–60	–55	
	At –60 dBFs		–20	–15	
Idle channel noise	20 Hz to 20 kHz, A-weighted, Gain = 0 dB		–85	–78	dBFs
	16 kHz: < 20 Hz to 7 kHz, Gain = 0 dB		–90		
	8 kHz: P-weighted voice, Gain = 18 dB		–87		
	16 kHz: < 20 Hz to 7 kHz, Gain = 18 dB		–82		
Crosstalk A/D to D/A	Gain = 0 dB		–80	–70	dB
Crosstalk path between two microphones		–70			dB
Intermodulation distortion	2-tone method			–60	dB
Input resistance differential(2)	Without ALC	50	70		kΩ
	With ALC	50	140		

(1) Gain range is defined by: Preamplifier = 0 to 30 dB; Filter = 0 to 31 dB (1-dB steps)
(2) The input resistance differential depends on fine gain setting controlled only by ALC.

5.2.7 Microphone Amplification Stage

These stages perform the single-to-differential conversion for single-ended inputs. Two programmable gains from 0 dB to 30 dB can be set:

- Automatic level control for main microphone or submicrophone input. The gain step is 1 dB.
- Level control by register for line-in or car-kit input, or headset microphone. The gain step is 6 dB.

The amplification stage outputs are connected to the ADC input (ADC left and right).

5.2.8 Digital Audio Filter Module

Figure 5-30 shows the digital audio filter uplink full path characteristics for the audio interface.

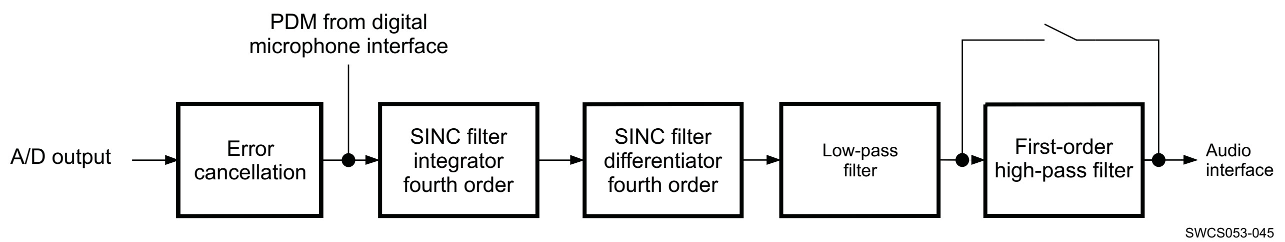


Figure 5-30. Digital Audio Filter Uplink Path Characteristics

The high-pass filter can be bypassed. It is controlled by register MISC_SET_2, address 0x49, ATX_HPF_BYP bit.

Table 5-21 shows the audio filter frequency response relative to reference gain at 1 kHz.

Table 5-21. Digital Audio Filter TX Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband		0.0005		0.42	F_S
Passband gain	In region 0.0005 × F_S to 0.42 × F_S (1)	–0.25		0.25	dB
Stopband			0.6		F_S
Stopband attenuation	In region 0.6 × F_S to 1 × F_S (1)		60		dB
Group delay			15.8/F_S		μs

(1) F_S is the sampling frequency (8, 11.025, 12, 16, 22.05, 24, 32, 44.1, or 48 kHz).

5.2.9 Digital Voice Filter Module

Figure 5-31 shows the digital voice filter uplink full path characteristics for the voice interface.

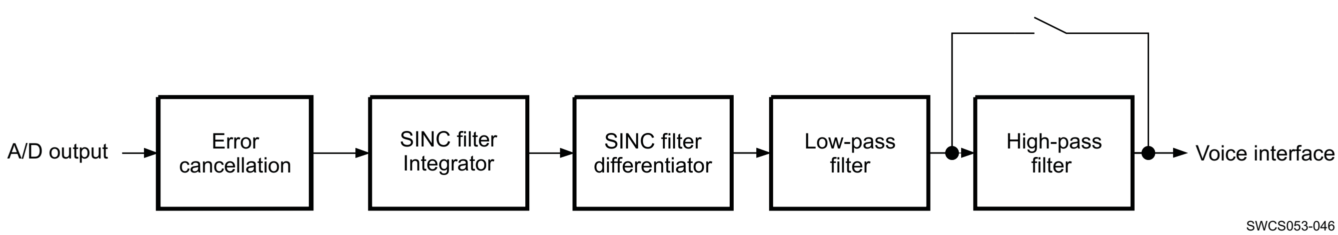


Figure 5-31. Digital Audio Filter Uplink Path Characteristics

The global high-pass filter or only the 3rd order high-pass filter can be bypassed (when 3rd order HPF is skipped, 1st order is still active). It is controlled by register MISC_SET_2, address 0x49, the VTX_3RD_HPF_BYP bit for the 3rd order high-pass filter, and the VTX_HPF_BYP bit for the global high-pass filter.

5.2.9.1 Voice Uplink Filter (with Sampling Frequency at 8 kHz)

Table 5-22 shows the voice filter frequency response relative to reference gain at 1 kHz with F_S = 8 kHz.

Table 5-22. Digital Voice Filter TX Electrical Characteristics with F_S = 8 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response relative to reference gain at 1 kHz	100 Hz			–20	dB
	200 Hz	–8		–0.5	
	300 Hz to 3300 Hz	–0.5	0	0.5	
	3400 Hz	–1.5	0	0.1	
	4000 Hz			–17	
	4600 Hz			–40	
	>6000 Hz			–45	
Pole when high-pass filter is disabled (1st order HPF)			24		Hz
Group delay			0.5		ms

Figure 5-32 and Figure 5-33 show the voice uplink frequency response with a sampling frequency of 8 kHz.

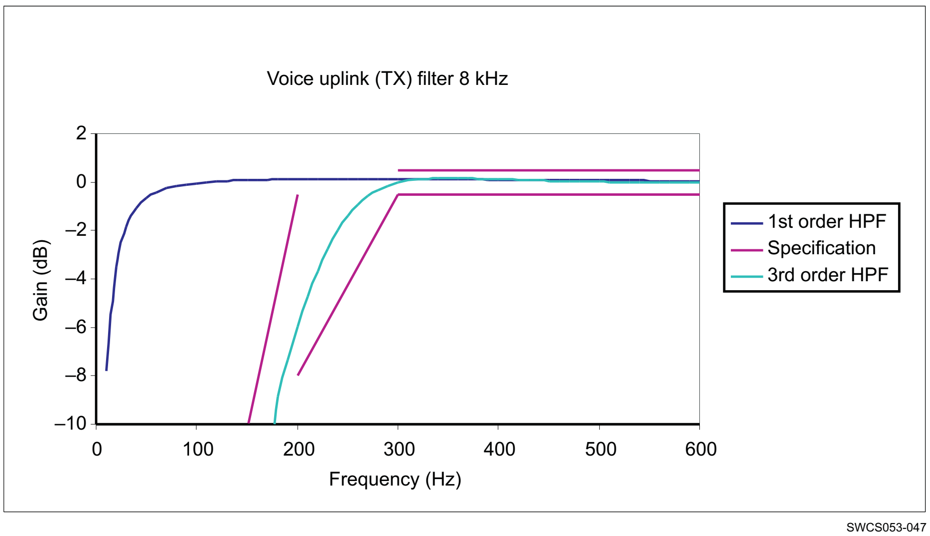


Figure 5-32. Voice Uplink Frequency Response with F_S = 8 kHz (Frequency Range 0 to 600 Hz)

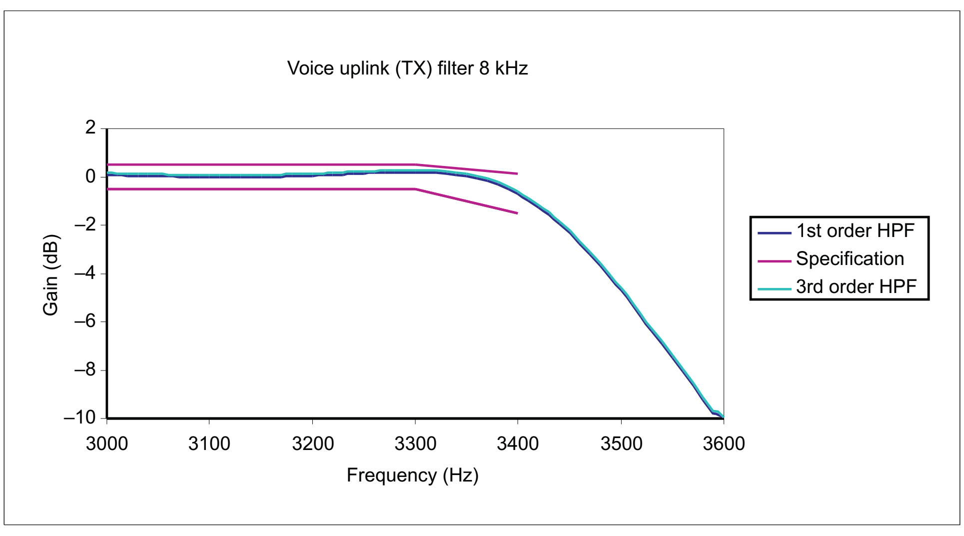


Figure 5-33. Voice Uplink Frequency Response with F_S = 8 kHz (Frequency Range 3000 to 3600 Hz)

5.2.9.2 Voice Uplink Filter (with Sampling Frequency at 16 kHz)

Table 5-23 shows the voice filter frequency response relative to reference gain at 1 kHz with F_S = 16 kHz.

Table 5-23. Digital Voice Filter TX Electrical Characteristics with F_S = 16 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response relative to reference gain at 1 kHz (1st order HPF)	300 Hz to 6600 Hz	–0.5		0.5	dB
	6800 Hz	–1.5		0.1	
	8000 Hz	–0.5	0	–17	
	9200 Hz	–1.5	0	–40	
	12000 Hz			–45	
Pole when 3rd order high-pass filter is disabled (1st order HPF)			47		Hz

Figure 5-34 and Figure 5-35 show the voice uplink frequency response with a sampling frequency of 16 kHz.

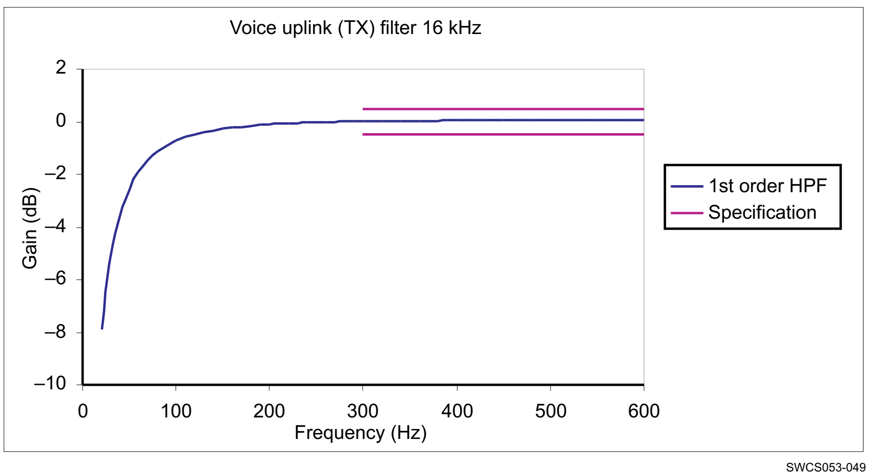


Figure 5-34. Voice Uplink Frequency Response with F_S = 16 kHz (Frequency Range 0 to 600 Hz)

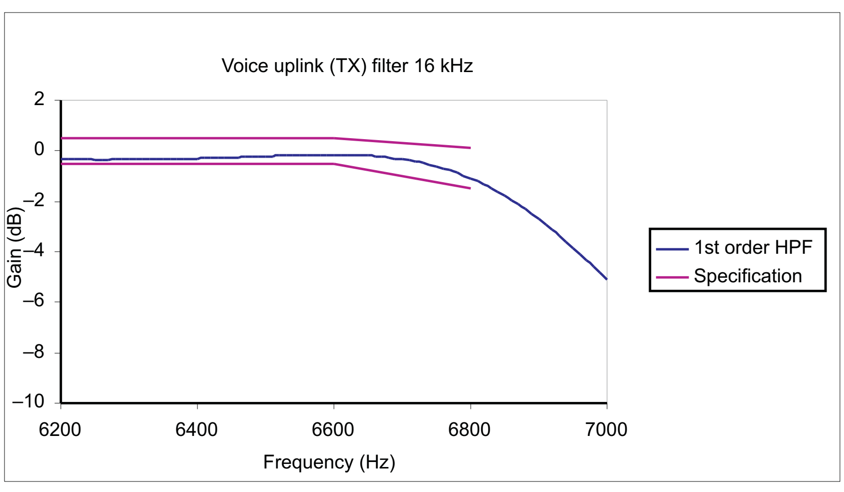


Figure 5-35. Voice Uplink Frequency Response with F_S = 16 kHz (Frequency Range 6200 to 7000 Hz)

6 Power Module

This chapter describes the electrical characteristics of the voltage regulators and timing characteristics of the supplies digitally controlled within the TPS65951.

Figure 6-1 shows the power provider block diagram.

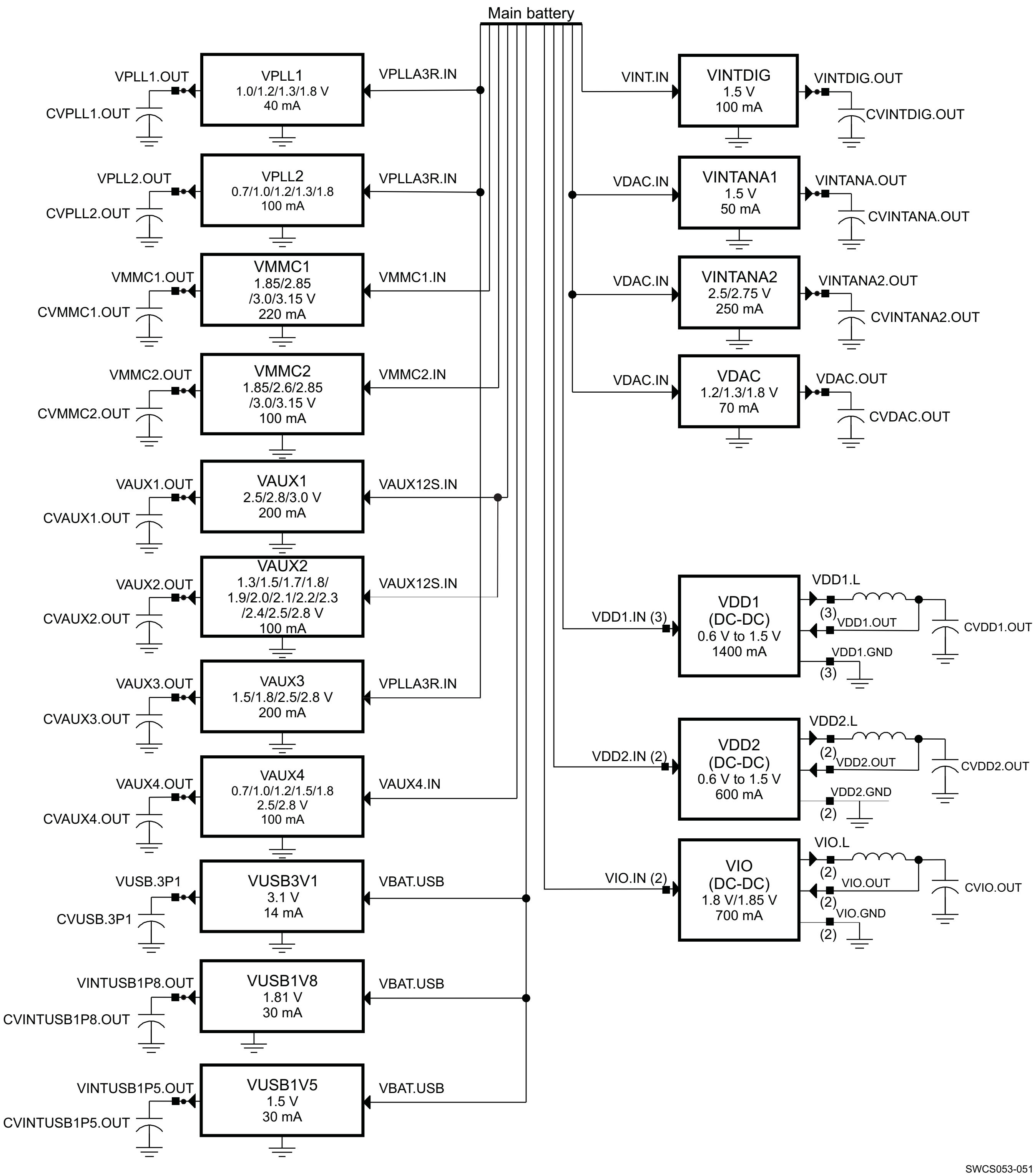


Figure 6-1. Power Provider Block Diagram

NOTE

For the component values, see Table 12-1, *TPS65951 External Components*.

6.1 Power Provider

Table 6-1. Summary of the Power Provider

NAME	USAGE	TYPE	VOLTAGE RANGE (V)	DEFAULT VOLTAGE DEPENDING ON BOOT MODE(1)				MAXIMUM CURRENT
				MC027S	MC027	MC021	SC021	
VAUX1	External	LDO	2.5, 2.8, 3.0	3.0 V	3.0 V	3.0 V	2.5 V	200 mA
VAUX2	External	LDO	1.3, 1.5, 1.7, 1.8, 1.9, 2.0, 2.1, 2.2, 2.3, 2.4, 2.5, 2.8	2.8 V	2.8 V	1.8 V	1.8 V	100 mA
VAUX3	External	LDO	1.5, 1.8, 2.5, 2.8	2.8 V	2.8 V	2.8 V	1.5 V	200 mA
VAUX4	External	LDO	0.7, 1.0, 1.2, 1.5, 1.8, 2.5, 2.8	1.2 V	1.2 V	2.8 V	2.5 V	100 mA
VMMC1	External	LDO	1.85, 2.85, 3.0, 3.15	1.85 V	1.85 V	3.0 V	3.0 V	220 mA
VMMC2	External	LDO	1.85, 2.6, 2.85, 3.0, 3.15	2.6 V	2.6 V	2.6 V	2.8 V	100 mA
VPLL1	External	LDO	1.0, 1.2, 1.3, 1.8	1.3 V	1.3 V	1.8 V	1.8 V	40 mA
VPLL2	External	LDO	0.7, 1.0, 1.2, 1.3, 1.8	1.2 V	1.3 V	1.3 V	1.3 V	100 mA
VDAC	External	LDO	1.2, 1.3, 1.8	1.8 V	1.8 V	1.8 V	1.8 V	70 mA
VIO	External	SMPS	1.8, 1.85	1.8 V	1.8 V	1.8 V	1.8 V	700 mA
VDD1	External	SMPS	0.6 ... 1.5	1.3 V	1.3 V	1.2 V	1.2 V	1400 mA
VDD2	External	SMPS	0.6 ... 1.5	1.3 V	1.3 V	1.2 V	1.2 V	600 mA
VINTANA1	Internal	LDO	1.5	1.5 V	1.5 V	1.5 V	1.5 V	50 mA
VINTANA2	Internal	LDO	2.5, 2.75	2.75 V	2.75 V	2.75 V	2.75 V	250 mA
VINTDIG	Internal	LDO	1.5	1.5 V	1.5 V	1.5 V	1.5 V	100 mA
USBCP	Internal	Charge Pump	5	5 V	5 V	5 V	5 V	100 mA
VUSB1V5	Internal	LDO	1.5	1.5 V	1.5 V	1.5 V	1.5 V	30 mA
VUSB1V8	Internal	LDO	1.8	1.8 V	1.8 V	1.8 V	1.8 V	30 mA
VUSB3V1	Internal	LDO	3.1	3.1 V	3.1 V	3.1 V	3.1 V	14 mA
VRRTC	Internal	LDO	1.5	1.5 V	1.5 V	1.5 V	1.5 V	30 mA
VBRTC	Internal	LDO	1.3	1.3 V	1.3 V	1.3 V	1.3 V	100 μA

(1) See Section 6.5 to understand the significance of the boot mode.

6.1.1 VDD1 DC-DC Regulator

6.1.1.1 VDD1 DC-DC Regulator Characteristics

The VDD1 DC-DC regulator is a stepdown DC-DC converter with a configurable output voltage. The programming of the output voltage and the characteristics of the DC-DC converter are SmartReflex compatible. The regulator can be put in sleep mode to reduce its leakage (PFM) or power-down mode when it is not being used. Table 6-2 describes the regulator characteristics.

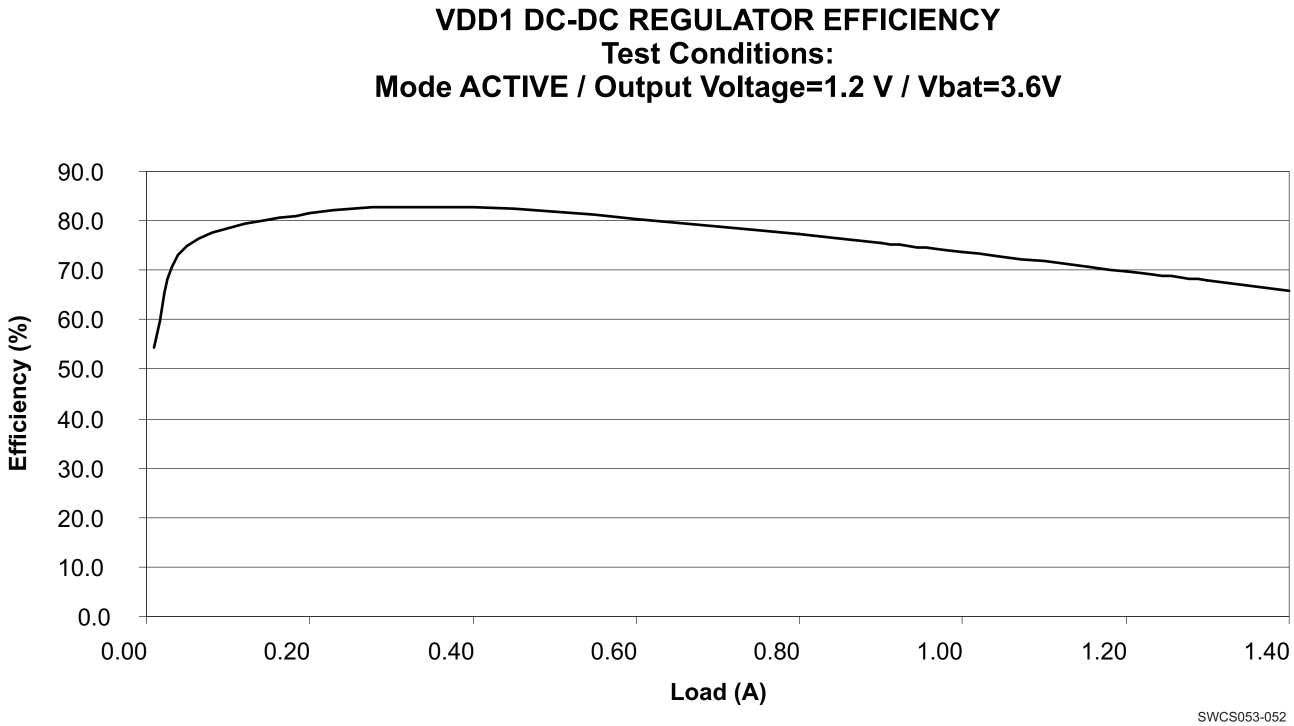
Table 6-2. VDD1 DC-DC Regulator Characteristics

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6		1.5	V
Output voltage step	Covering the 0.6-V to 1.5-V range		12.5		mV
Output accuracy(1)	0.6 V to < 0.8 V	–6%		6%	
	0.8 V to 1.5 V	–5%		5%	
Switching frequency, see Table 6-21			3.2		MHz
Conversion efficiency(2), Figure 6-2 in active mode and Figure 6-3 in sleep mode	I_O = 10 mA, Sleep		82%		
	100 mA < I_O < 400 mA		85%		
	400 mA < I_O < 600 mA		80%		
	600 mA < I_O < 800 mA		75%		
Output current	Active mode, output voltage = 0.6 V to 1.2 V			1.2	A
	Active mode, output voltage = 1.2 V to 1.5 V			1.4	A
	Sleep mode			10	mA
Ground current (I_Q)	Off at 30°C			3	µA
	Sleep, unloaded		30	50	
	Active, unloaded, not switching			300	
Short-circuit current	$V_{IN} = V_{MAX}$		2.2		A
Load regulation	$0 < I_O < I_{MAX}$			20	mV
Transient load regulation(3)	I_O = 10 mA to 400 + 10 mA, Maximum slew rate is 400 mA/100 ns	–65		50	mV
Line regulation				10	mV
Transient line regulation	300 mV_{PP} ac input, 10-µs rise and fall time			10	mV
Start-up time			0.25	1	ms
Recovery time	From sleep to on with constant load		< 10	100	µs
Slew rate (rising or falling)(4)		4	8	16	mV/µs
Output ripple	Active (PWM and PSM)	–10		10	mV
	Sleep (PFM)	–2%		2%	
Current limit for PWM/PSM mode switch. PSM is below this limit, and PWM is above this limit.	Active mode	150		200	mA
Overshoot	softstart			5%	
Output pulldown resistance	In off mode		500	700	Ω
External coil	Value	0.7	1	1.3	µH
	DCR			0.1	Ω
	Saturation current for 1.2-A operation	1.8			A
	Saturation current for 1.4-A operation	2.1			
External capacitor(5)	Value	5	10	15	µF
	ESR at switching frequency	0		20	mΩ

(1) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process)
(2) VBAT = 3.8 V, VDD1 = 1.3 V, Fs = 3.2 MHz, L = 1 µH, L_{DCR} = 100 mΩ, C = 10 µF, ESR = 10 mΩ
(3) Output voltage needs to be able to discharge the load current completely and settle to its final value within 100 µs.
(4) Load current varies proportional to the output voltage. The slew rate is for both increasing and decreasing voltages and the maximum load current is 1.1 A.
(5) Under current load condition step:
400 mA in 100 ns with a ±50% external capacitor accuracy or
Transient load condition can be improved to Imax/2 with a more accurate capacitor value, that is:
600 mA in 100 ns with a ±20% external capacitor accuracy.

When the VDD1 DC-DC converter is not used, there are no issues with current, voltage, and stress under nominal conditions. See Table 2-3 on how to connect the VDD1/2 DC-DC converter when it is not in use.

Figure 6-2 and Figure 6-3 show the efficiency of the VDD1 DC-DC regulator in active mode and in sleep mode, respectively.



NOTE: The efficiency measurements are done on a part in a socket, which degrades the efficiency by a few %-units.

Figure 6-2. VDD1 DC-DC Regulator Efficiency in Active Mode

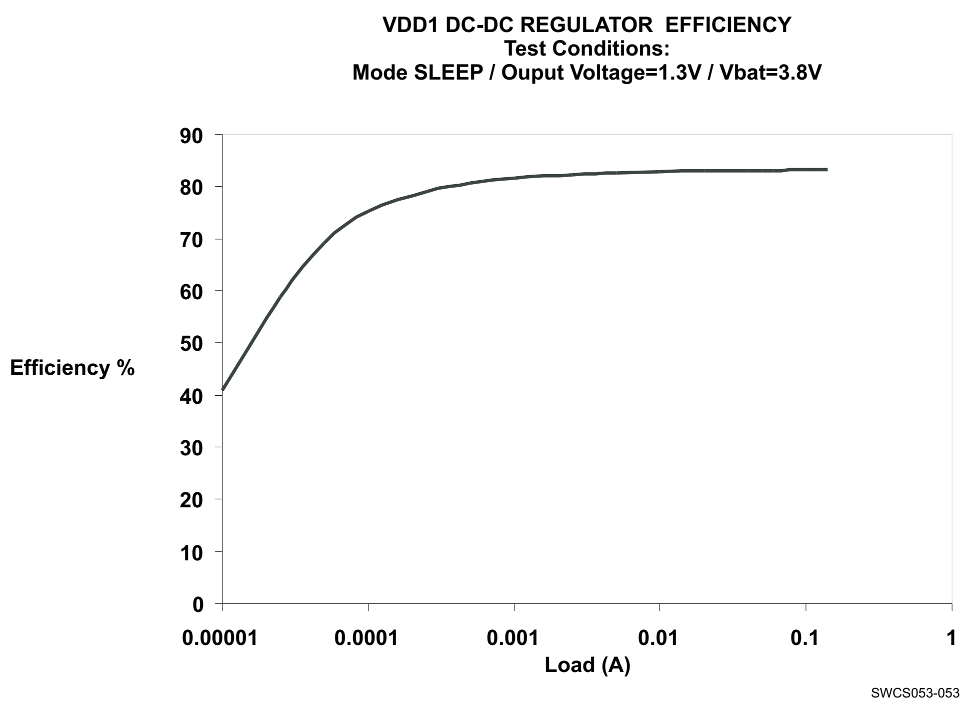


Figure 6-3. VDD1 DC-DC Regulator Efficiency in Sleep Mode

6.1.1.2 External Components and Application Schematics

Figure 6-4 shows the application schematic with the external components on the VDD1 DC-DC regulator.

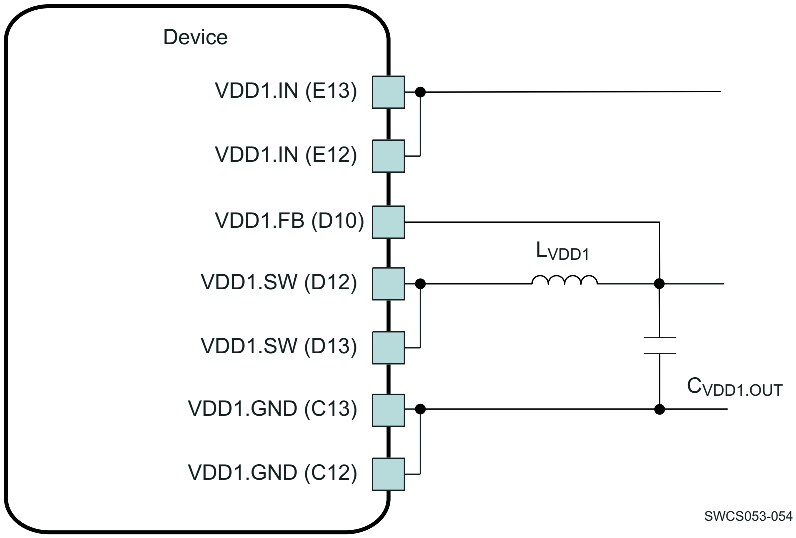


Figure 6-4. VDD1 DC-DC Application Schematic

NOTE

For the component values, see Table 12-1, *TPS65951 External Components*.

6.1.2 *VDD2 DC-DC Regulator*

6.1.2.1 VDD2 DC-DC Regulator Characteristics

The VDD2 DC-DC regulator is a programmable output stepdown DC-DC converter with an internal FET. Like the VDD1 regulator, the VDD2 regulator can be placed in sleep or power-down mode and is SmartReflex compatible. The VDD2 regulator differs from VDD1 in its current load capability. Table 6-3 describes the regulator characteristics.

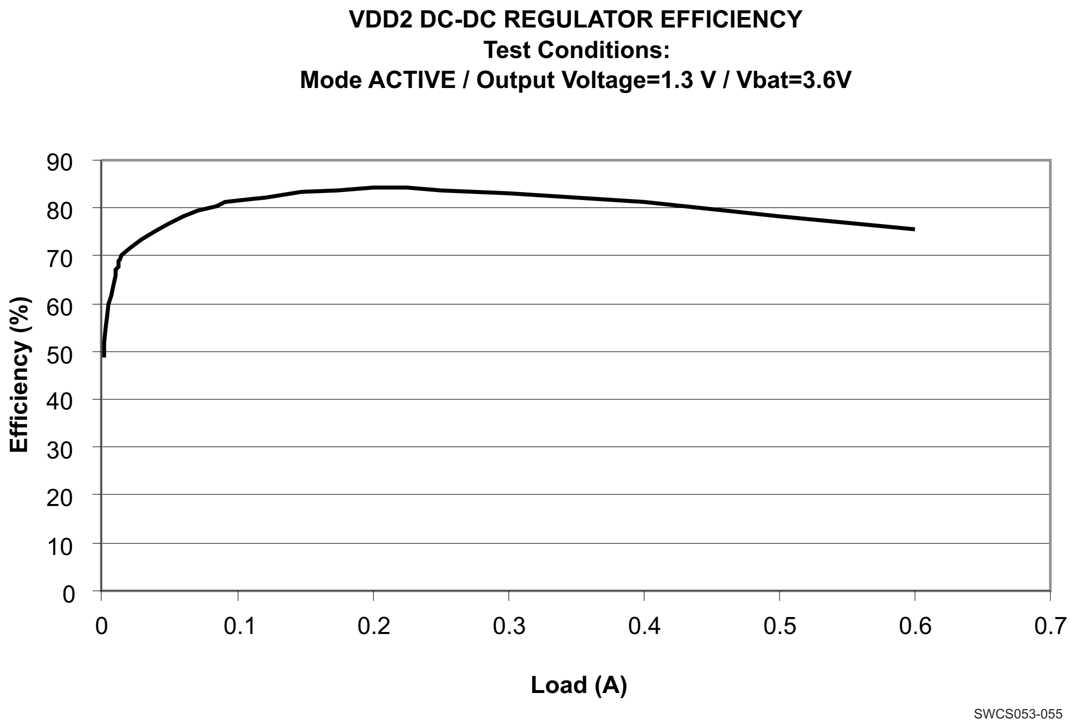
Table 6-3. VDD2 DC-DC Regulator Characteristics

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6	1	1.5	V
Output voltage step	Covering the 0.6-V to 1.5-V range,		12.5		mV
Output accuracy(1)	0.6 V to < 0.8 V	–6%		6%	
	0.8 V to 1.5 V	–5%		5%	
Switching frequency(2), see Table 6-21			3.2		MHz
Conversion efficiency(3), Figure 6-5 in active mode and Figure 6-6 in sleep mode	I_O = 10 mA, Sleep		82%		
	100 mA < I_O < 300 mA		85%		
	300 mA < I_O < 500 mA		80%		
Output current	Active mode			600	mA
	Sleep mode			10	mA
Ground current (I_Q)	Off at 30°C			1	µA
	Sleep, unloaded			50	
	Active, unloaded, not switching			300	
Short-circuit current	V_{IN} = V_{MAX}		1.2		A
Load regulation	0 < I_O < I_{MAX}			20	mV
Transient load regulation(4)	I_O = 10 mA to (I_{MAX}/3) + 10 mA, Maximum slew rate is I_{MAX}/3/100 ns	–65		50	mV
Line regulation				10	mV
Transient line regulation	300 mV_{PP} ac input, 10-µs rise and fall time			10	mV
Output pulldown resistance	In off mode		500	700	Ω
Start-up time			0.25	1	ms
Recovery time	From sleep to on with constant load		25	100	µs
Slew rate (rising or falling)(5)		4	8	16	mV/µs
Output ripple	Active (PWM & PSM)	–10		10	mV
	Sleep (PFM)	–2%		2%	
Current limit for PWM/PSM mode switch. PSM is below this limit, and PWM is above this limit.		150		200	mA
Overshoot	softstart			5%	
External coil	Value	0.7	1	1.3	µH
	DCR			0.1	Ω
	Saturation current	900			mA
External capacitor(6)	Value	5	10	15	µF
	ESR at switching frequency	0		20	mΩ

(1) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process)
(2) 2 modes are available:
Mode1: VDD2 switcher uses its own RC oscillator clock (default).
Mode2: VDD2 switcher could be configured to use clock from VIO clock (based on HFCLKIN input clock).
(3) VBAT = 3.8 V, VDD2 = 1.3 V, Fs = 3.2 MHz, L = 1 µH, L_{DCR} = 100 mΩ, C = 10 µF, ESR = 10 mΩ
(4) Output voltage needs to be able to discharge the load current completely and settle to its final value within 100 µs.
(5) Load current varies proportional to the output voltage. The slew rate is for both increasing and decreasing voltages and the maximum load current is 600 mA.
(6) Under current load condition step:
Imax/3 (200 mA) in 100 ns with a ±50% external capacitor accuracy or
Transient load condition can be improved to Imax/2 with a more accurate capacitor value, that is:
Imax/2 (300 mA) in 100 ns with a ±20% external capacitor accuracy.

When the VDD2 DC-DC converter is not used, there are no issues with current, voltage, and stress under nominal conditions. See Table 2-3 on how to connect the VDD1/2 DC-DC converter when it is not in use.

Figure 6-5 and Figure 6-6 show the efficiency of the VDD1 DC-DC regulator in active mode and in sleep mode, respectively.



NOTE: The efficiency measurements are done on a part in a socket, which degrades the efficiency by a few %-units.

Figure 6-5. VDD2 DC-DC Regulator Efficiency in Active Mode

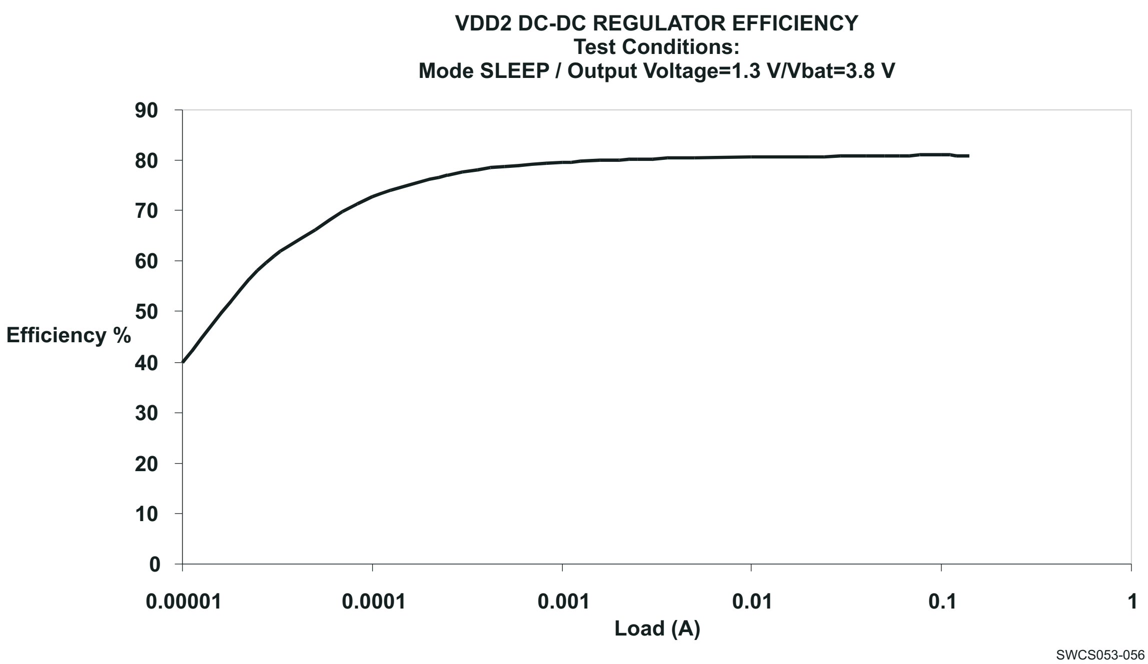


Figure 6-6. VDD2 DC-DC Regulator Efficiency in Sleep Mode

6.1.2.2 External Components and Application Schematics

Figure 6-7 shows the application schematic with the external components on the VDD2 DC-DC regulator.

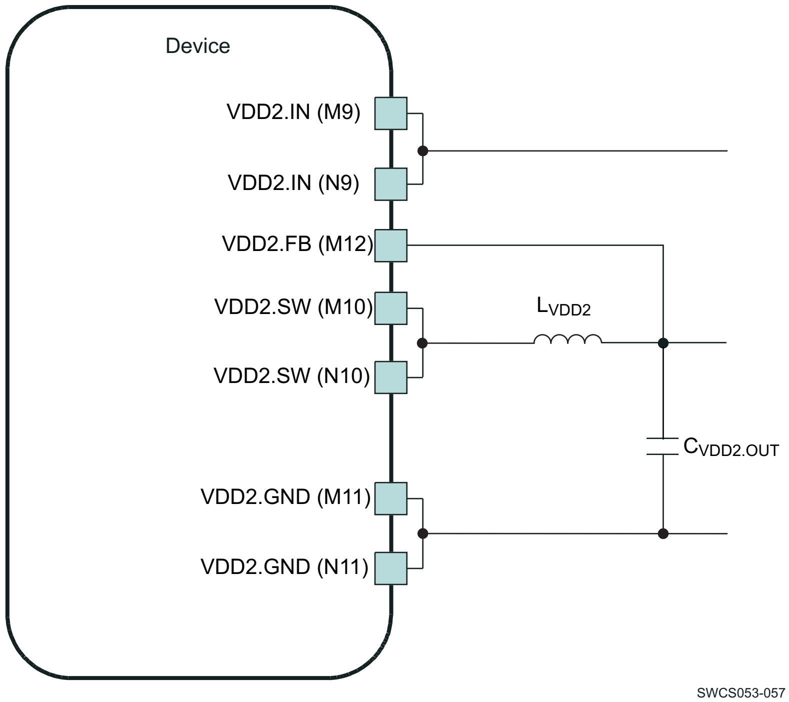


Figure 6-7. VDD2 DC-DC Application Schematic

NOTE

For the component values, see Table 12-1, *TPS65951 External Components*.

6.1.3 VIO DC-DC Regulator

6.1.3.1 VIO DC-DC Regulator Characteristics

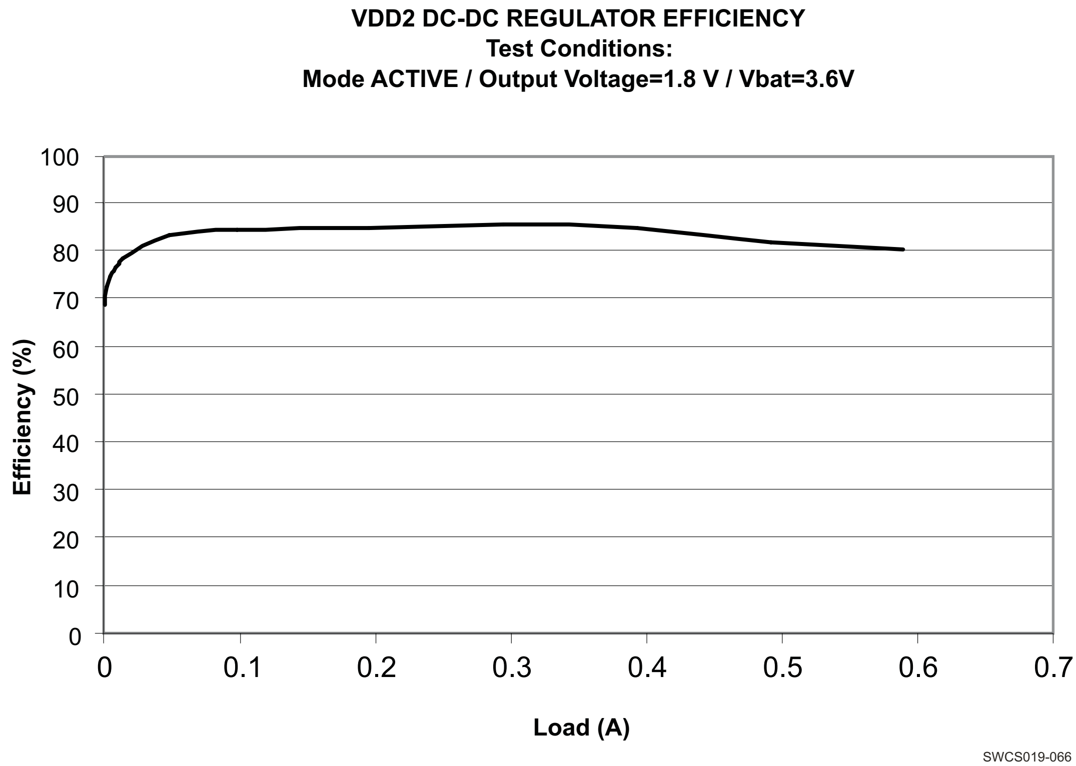
The I/Os and memory DC-DC regulator is a 700-mA stepdown DC-DC converter (internal FET) with a choice of two output voltage settings. It supplies the memories and all I/O ports in the application and is one of the first power providers to switch on in the power-up sequence. This DC-DC regulator can be placed sleep or power-down mode; however, care must be taken in the sequencing of this power provider as numerous ESD blocks are connected to this supply. Table 6-4 describes the regulator characteristics.

Table 6-4. VIO DC-DC Regulator Characteristics

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
Input voltage range		2.7	3.6	4.5	V
Output voltage(1)			1.8 1.85		V
Output accuracy (2)		–3%		3%	
		–4%		4%	
Switching frequency(3), see Table 6-21			3.2		MHz
Conversion efficiency(4) Figure 6-8 in active mode and Figure 6-9 in sleep mode	I_O = 10 mA, Sleep		85%		
	100 mA < I_O < 400 mA		85%		
	400 mA < I_O < 600 mA		80%		
Output current(5)	On mode			700	mA
	Sleep mode			10	
Ground current (I_Q)	Off at 30°C			1	μA
	Sleep, unloaded			50	
	Active, unloaded, not switching			300	
Load regulation	0 < I_O < I_{MAX}			20	mV
Line regulation				10	mV
Load transient and line transient (cumulated)	I_O = 10 mA to 150 mA in dt = 100 ns I_O = 150 mA to 250 mA in dt = 100 ns I_O = 250 mA to 450 mA in dt = 100 ns 600 mV_{PP} ac, input rise and fall time 10 μs			40	mV
Start-up time			0.25	1	ms
Recovery time	From sleep to on with constant load		< 10	100	μs
Output ripple	Active (PWM & PSM)	–10		10	mV
	Sleep (PFM)	–2%		2%	
Current limit for PWM/PSM mode switch. PSM is below this limit, and PWM is above this limit.		150		200	mA
Overshoot	softstart			5%	
Output pulldown resistance	In off mode		500	700	Ω
External coil	Value	0.7	1	1.3	μH
	DCR			0.1	Ω
	Saturation current	900			mA
External capacitor	Value	5	10	15	μF
	ESR at switching frequency	1		20	mΩ

(1) This voltage is tuned according to the platform and transient requirements.
(2) ±4% accuracy includes all the variation (line and load regulation, line and load transient, temperature, process)
±3% accuracy is DC accuracy only.
(3) 2 modes are available:
Mode1: VIO switcher uses its own RC oscillator clock (default).
Mode2: VIO switcher could be configured to use clock from VIO clock (based on HFCLKIN input clock).
(4) VBAT = 3.8 V, VIO = 1.8 V, Fs = 3.2 MHz, L = 1 μH, L_{DCR} = 100 mΩ, C = 10 μF, ESR = 10 mΩ
(5) Typical VIO internal current consumption is 5 mA during USB data transfer.

Figure 6-8 and Figure 6-9 show the efficiency of the VIO DC-DC regulator in active mode and in sleep mode, respectively.



NOTE: The efficiency measurements are done on a part in a socket, which degrades the efficiency by a few %-units.

Figure 6-8. VIO DC-DC Regulator Efficiency in Active Mode

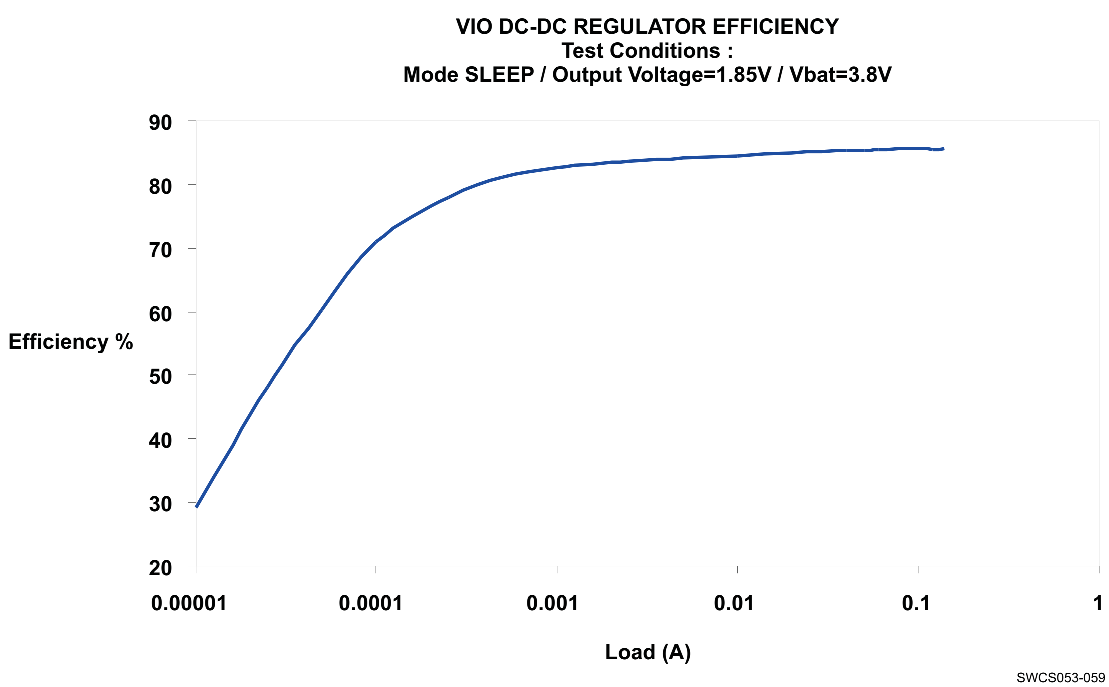


Figure 6-9. VIO DC-DC Regulator Efficiency in Sleep Mode

6.1.3.2 External Components and Application Schematics

Figure 6-10 shows the application schematic with the external components on the VIO DC-DC regulator.

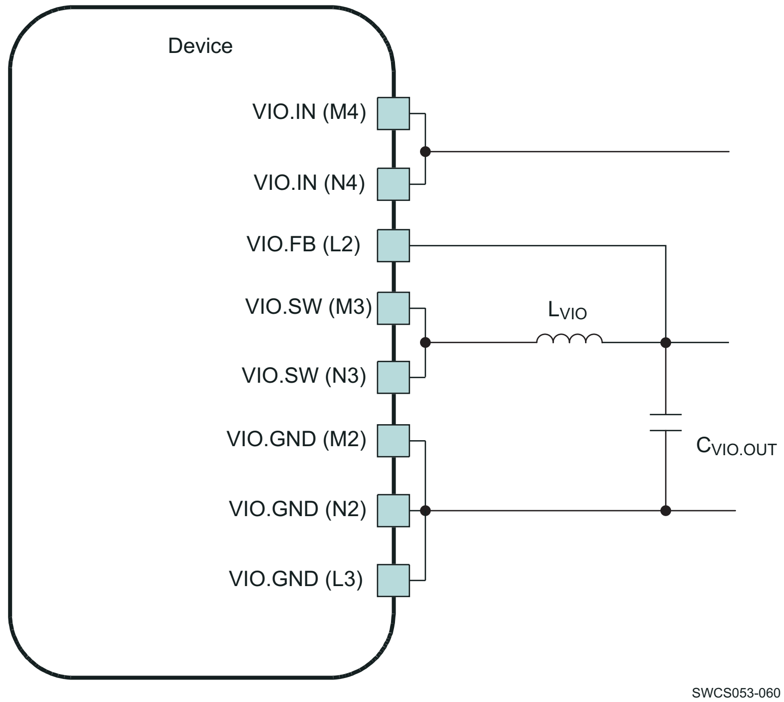


Figure 6-10. VIO DC-DC Application Schematic

NOTE

For the component values, see Table 12-1, *TPS65951 External Components*.

6.1.4 VDAC LDO Regulator

The VDAC programmable LDO regulator is a high-PSRR, low-noise, linear regulator that powers the host processor dual-video DAC. It is controllable with registers via I^2C and can be powered down. Table 6-5 describes the regulator characteristics.

Table 6-5. VDAC LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VDAC.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage(2)		1.164	1.2	1.236	V
			1.261	1.3	1.339	
			1.746	1.8	1.854	
I_{OUT}	Rated output current	On mode			70	mA
		Low-power mode			5	
	DC load regulation	On mode: $0 < I_O < I_{MAX}$			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 20 kHz	65			dB
		20 kHz < f < 100 kHz	45			
		f = 1 MHz	40			
		$V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$				
	Output noise	200 Hz < f < 5 kHz			400	nV/√Hz
		5 kHz < f < 400 kHz			125	
		400 kHz < f < 10 MHz			50	
	Ground current	On mode, $I_{OUT} = 0$			150	μA
		On mode, $I_{OUT} = I_{OUTmax}$			350	
		Low-power mode, $I_{OUT} = 0$			15	
		Low-power mode, $I_{OUT} = 1$ mA			25	
		Off mode at 55°C			1	
V_{DO}	Dropout voltage(3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 60 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.5 VPLL1 LDO Regulator

The VPLL1 programmable LDO regulator is high-PSRR, low-noise, linear regulator used for the host processor PLL supply. Table 6-6 describes the regulator characteristics.

Table 6-6. VPLL1 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VPLL1.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage(2)		0.97	1.0	1.03	V
			1.164	1.2	1.236	
			1.261	1.3	1.339	
			1.746	1.8	1.854	
I_{OUT}	Rated output current	On mode			40	mA
		Low-power mode			5	
	DC load regulation	On mode: $0 < I_O < I_{MAX}$			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz	50			dB
		10 kHz < f < 100 kHz	40			
		f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	30			
	Ground current	On mode, $I_{OUT} = 0$			70	µA
		On mode, $I_{OUT} = I_{OUTmax}$			110	
		Low-power mode, $I_{OUT} = 0$			15	
		Low-power mode, $I_{OUT} = 1$ mA			16	
		Off mode at 55°C			1	
V_{DO}	Dropout voltage(3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 60 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.6 VPLL2 LDO Regulator

The VPLL2 programmable LDO regulator is a high-PSRR, low-noise, linear regulator used for the host processor PLL supply. Table 6-7 describes the regulator characteristics.

Table 6-7. VPLL2 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VPLL2.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage(2)		0.672 0.97 1.164 1.261 1.746	0.7 1.0 1.2 1.3 1.58	0.728 1.03 1.236 1.339 1.854	V
I_{OUT}	Rated output current	On mode Low-power mode			100 5	mA
	DC load regulation	On mode: $0 < I_O < I_{MAX}$			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	50 40 30			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 1$ mA Off mode at 55°C			70 160 17 20 1	µA
V_{DO}	Dropout voltage(3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.7 VMMC1 LDO Regulator

The VMMC1 LDO regulator is a programmable linear voltage converter that powers the MMC slot. It includes a discharge resistor and overcurrent protection (short-circuit). This LDO regulator can also be turned off automatically when the MMC card extraction is detected (through one dedicated GPIO, description in TRM). The VMMC1 LDO can be powered via an independent supply other than the battery; for example, a charge pump. In this case, the input from the VMMC1 LDO can possibly be higher than the battery voltage. Table 6-8 describes the regulator characteristics.

Table 6-8. VMMC1 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VMMC1.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	5.5	V
V_{OUT}	Output voltage(2)		1.7945 2.7645 2.91 3.0555	1.85 2.85 3.0 3.15	1.9055 2.9355 3.09 3.2445	V
I_{OUT}	Rated output current	On mode Low-power mode			220 5	mA
	DC load regulation	On mode: $0 < I_O < I_{MAX}$			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	50 40 25			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 290 17 20 1	μA
V_{DO}	Dropout voltage(3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.8 VMMC2 LDO Regulator

The VMMC2 LDO regulator is a programmable linear voltage converter that powers the MMC slot 2. It includes a discharge resistor and overcurrent protection (short-circuit). This LDO regulator can also be turned off automatically when the MMC card extraction is detected (through one dedicated GPIO, description in TRM). The VMMC2 LDO can be powered via an independent supply other than the battery; for example, a charge pump. In this case, the input from the VMMC2 LDO can possibly be higher than the battery voltage. Table 6-9 describes the regulator characteristics.

Table 6-9. VMMC2 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VMMC2.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	5.5	V
V_{OUT}	Output voltage(2)		1.795 2.522 2.765 2.91 3.056	1.85 2.6 2.85 3.0 3.15	1.906 2.678 2.936 3.09 3.245	V
I_{OUT}	Rated output current	On mode Low-power mode			100 5	mA
	DC load regulation	On mode: $0 < I_O < I_{MAX}$			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	50 40 30			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 50$ µA Off mode at 55°C			70 170 17 20 1	µA
V_{DO}	Dropout voltage(3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.9 VAUX1 LDO Regulator

The VAUX1 general-purpose LDO regulator powers the auxiliary devices. The VAUX1 regulator can also support an inductive load such as a vibrator. While operating in vibrator mode, it has the following features:

- Programmable, register-controlled, soft-start function
- Enable via VIBRA.SYNC pin
- Programmable, register-controlled, duty cycle (PWM generator) based on a nominal 4-Hz cycle which is derived from an internal 32-kHz clock.

Table 6-10 describes the regulator characteristics.

Table 6-10. VAUX1 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VAUX1.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
	Vibrator inductive load(2)	Connected from VAUX1.OUT to analog ground	70		700	µH
	Vibrator load resistance(2)		15		50	Ω
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage(3)		2.425 2.716 2.91	2.5 2.8 3.0	2.575 2.884 3.09	V
I_{OUT}	Rated output current	On mode Low-power mode			200 5	mA
	DC load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT}) Soft-start function for inductive load			100 500	µs
	Turn-off time				5000	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	50 40 25			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 270 18 20 1	µA
V_{DO}	Dropout voltage(4)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(5)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Parameter not tested, used for design specification only
(3) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(4) For nominal output voltage
(5) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.10 VAUX2 LDO Regulator

The VAUX2 general-purpose LDO regulator powers the auxiliary devices. Table 6-11 describes the regulator characteristics.

Table 6-11. VAUX2 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VAUX2.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage(2)		–3%	1.3 1.5 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.8	+3%	V
I_{OUT}	Rated output current	On mode Low-power mode			100 5	mA
	DC load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	50 40 30			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 170 17 20 1	μA
V_{DO}	Dropout voltage(3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω
		Configurable as HighZ in off mode	100			MΩ

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.11 VAUX3 LDO Regulator

The VAUX3 general-purpose LDO regulator powers the auxiliary devices. Table 6-12 describes the regulator characteristics.

Table 6-12. VAUX3 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VAUX3.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage(2)		1.455 1.746 2.425 2.716	1.5 1.8 2.5 2.8	1.545 1.854 2.575 2.884	V
I_{OUT}	Rated output current	On mode Low-power mode			200 5	mA
	DC load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	50 40 25			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 270 15 20 1	μA
V_{DO}	Dropout voltage(3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.12 VAUX4 LDO Regulator

The VAUX4 general-purpose LDO regulator powers the auxiliary devices. The VAUX4 regulator has an independent supply input pin and can be preregulated by an external voltage. Table 6-13 describes the regulator characteristics.

Table 6-13. VAUX4 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VAUX4.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage	Under minimum dropout voltage condition	2.7	3.6	4.5	V
		V_{OUT} = 2.8 V I_{OUT} max = 6 mA	3.0	3.6	4.5	
V_{OUT}	Output voltage(2)		0.672 0.97 1.164 1.455 1.746 2.425 2.716	0.7 1.0 1.2 1.5 1.8 2.5 2.8	0.728 1.03 1.236 1.545 1.854 2.575 2.884	V
I_{OUT}	Rated output current	On mode Low-power mode			100 5	mA
	DC load regulation	On mode: I_{OUT} = I_{OUTmax} to 0			20	mV
	DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} at I_{OUT} = I_{OUTmax}			3	mV
	Turn-on time	I_{OUT} = 0, C_L = 1 µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz V_{IN} = V_{OUT} + 1 V, I_O = I_{MAX}	50 40 30			dB
	Ground current	On mode, I_{OUT} = 0 On mode, I_{OUT} = I_{OUTmax} Low-power mode, I_{OUT} = 0 Low-power mode, I_{OUT} = 5 mA Off mode at 55°C			70 170 17 20 1	µA
V_{DO}	Dropout voltage(3)	On mode, I_{OUT} = I_{OUTmax}			250	mV
		On mode, I_{OUT} = [0..6 mA], V_{OUTtyp} = 2.8 V			100	
	Transient load regulation(4)	I_{LOAD}: I_{MIN} – I_{MAX} Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.13 VINTDIG LDO Regulator

The VINTDIG LDO regulator supplies the TPS65951 digital blocks. Table 6-14 describes the regulator characteristics.

Table 6-14. VINTDIG LDO Regulator Characteristics (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VINTDIG.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage (2)		1.455	1.5	1.545	V
I_{OUT}	Rated output current	On mode Low-power mode			100 5	mA
	DC load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	50 40 30			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 1$ mA Off mode at 55°C			70 160 17 20 1	μA
V_{DO}	Dropout voltage (3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation (4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.14 VINTANA1 LDO Regulator

To supply the TPS65951 analog blocks, there are two LDOs: VINTANA1 (1.5 V) and VINTANA2 (2.75 V / 2.5 V). The 2.5-V setting is selected when the battery voltage falls below 3.0 V. Table 6-15 describes the regulator characteristics.

Table 6-15. VINTANA1 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VINTANA1.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage(2)		1.455	1.5	1.545	V
I_{OUT}	Rated output current	On mode Low-power mode			50 5	mA
	DC load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	65 45 40			dB
	Output noise	200 Hz < f < 5 kHz 5 kHz < f < 400 kHz 400 kHz < f < 10 MHz			400 125 50	nV/√Hz
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 1$ mA Off mode at 55°C			100 250 15 25 1	μA
V_{DO}	Dropout voltage(3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.15 VINTANA2 LDO Regulator

To supply the TPS65951 analog blocks, there are two LDOs: VINTANA1 (1.5 V) and VINTANA2 (2.75 V / 2.5 V). The 2.5-V setting is selected when the battery voltage falls below 3.0 V. Table 6-16 describes the regulator characteristics.

Table 6-16. VINTANA2 LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VINTANA2.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage(2)	2.7 V < VBAT < 3 V VBAT ≥ 3 V	2.425 2.6675	2.5 2.75	2.575 2.8325	V
I_{OUT}	Rated output current	On mode Low-power mode			250 5	mA
	DC load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 20 kHz 20 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	65 45 40			dB
	Output noise	200 Hz < f < 5 kHz 5 kHz < f < 400 kHz 400 kHz < f < 10 MHz			400 125 50	nV/√Hz
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 1$ mA Off mode at 55°C			150 450 15 25 1	μA
V_{DO}	Dropout voltage(3)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(4)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.16 VUSB3V1 Regulator

The VUSB3V1 internal LDO regulator powers the USB PHY, charger detection, and OTG of the USB subchip inside the TPS65951. Table 6-17 describes the regulator characteristics.

It can take its power from three possible sources (see Figure 6-11):

- VBAT (only for high battery voltages)
- VBUS (only in low-power mode)
- VUSBIN.CPOUT (PAD shared with CP.OUT)

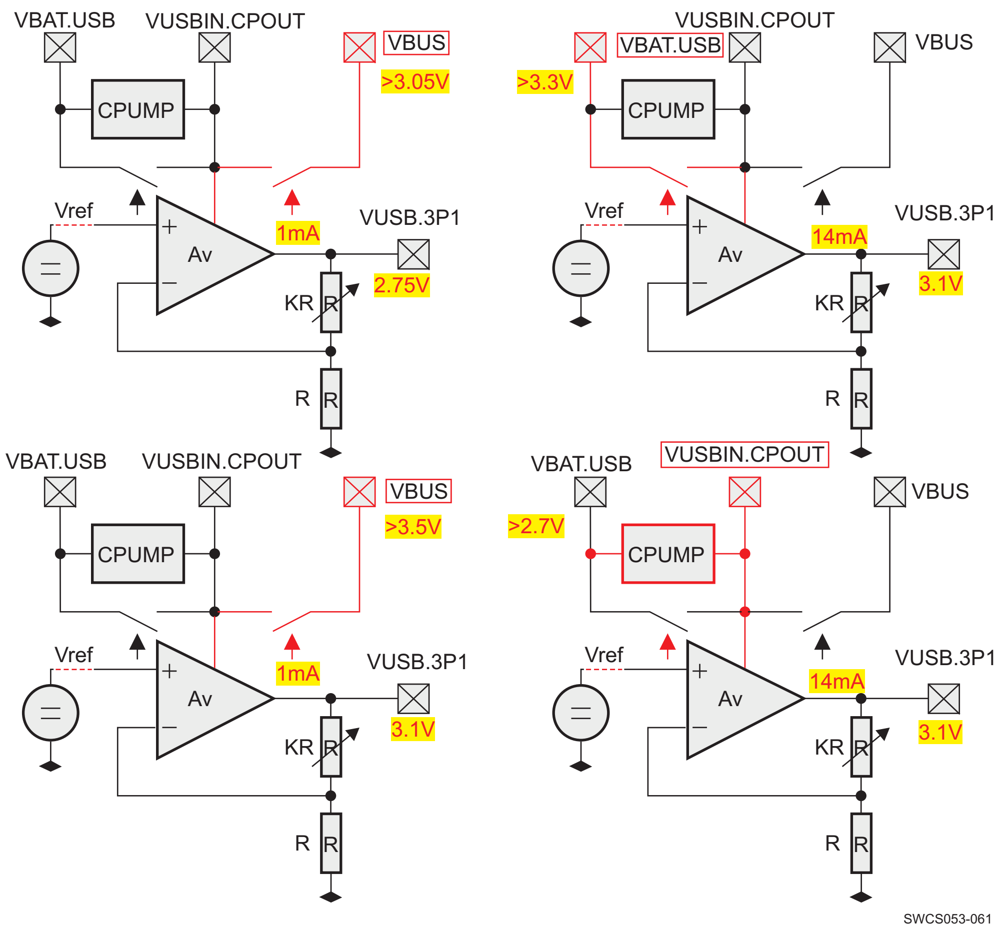


Figure 6-11. VUSB3V1 LDO Supply Selection for the Different Modes of Operation

USB standard requires data lines to be biased with pullups biased from a > 3.0-V supply, USB PHY cannot directly operate from battery for battery voltages lower than 3.3 V.

VUSBIN.CPOUT must be supplied by a boosted voltage in order to assure enough overhead for USB LDO operation. The internal charge pump (with output connected to VUSBIN.CPOUT) can be used for this purpose.

In order to select between these three power sources, a power multiplexer is connected to the VUSB3V1 LDO supply.

Table 6-17. VUSB3V1 Internal LDO Regulator Characteristics(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS					
Filtering capacitor	Connected between VUSB.3P1 and GND	0.5	2.2	2.7	µF
Filtering capacitor ESR		0	10	600	mΩ
ELECTRICAL CHARACTERISTICS					
Input voltage: $VIN_{VRUSB3V1}$	VBAT.USB	VOUTtyp + 0.2	3.6	4.5	V
	VUSB.IN	VOUTtyp + 0.2	5.0	5.25	V
	VBUS Sleep mode Precharge mode (VBUSdetect is VBUS comparator threshold from battery charger section)	VOUTtyp + 0.4 VBUSdetect	5.0 5.0	20 20	V
Output voltage(2): $V_{VRUSB3V1}$	On mode – VSEL = 001 On mode – VSEL = 010 On mode – VSEL = 011 On mode – VSEL = 000 (default) On mode – VSEL = 100 On mode – VSEL = 101 On mode – VSEL = 110 On mode – VSEL = 111 Precharge mode	2.55 2.65 2.75 3.00 3.10 3.20 3.30 3.40 2.55	2.65 2.75 2.85 3.10 3.20 3.30 3.40 3.50 2.78	2.80 2.90 3.00 3.20 3.30 3.40 3.50 3.60 3.00	V
Rated output current: $I_{VRUSB3V1}$	VBAT.USB/VUSBIN.CPOUT On mode Sleep mode			14 1	mA
	VBUS Precharge mode Sleep mode			1 1	mA
DC load regulation (On mode)	$V_{VRUSB3V1max} – V_{VRUSB3V1min}$; $0 < I_{VRUSB3V1} < 14$ mA			20	mV
DC line regulation (On mode)	$V_{VRUSB3V1min} – V_{VRUSB3V1max}$, $I_{VRUSB3V1max} = 14$ mA			20	mV
Turn-on time	$I_{VRUSB3V1min} = 0$, $C_{VRUSB3V1} = 1$ µF, $V_{VRUSB3V1} = V_{VRUSB3V1final}$ ±1%			1	ms
Turn-off time	$I_{VRUSB3V1max} = 14$ mA, $C_{VRUSB3V1} = 2.7$ µF			5	ms
Ripple rejection (On mode)	$I_{VRUSB3V1max} = 14$ mA, $VIN_{VRUSB3V1} = 3.3$ V f < 100 Hz 100 Hz < f < 1 MHz f > 1 MHz	 50 30 20			dB
Ground current	Consumption, Off, $I_{VUSB3V1} = 0$ — IVBAT(3)			5	µA
	Sleep, $I_{VUSB3V1} = 0$ — IVBAT(3)			45	µA
	On mode, $I_{VUSB3V1} = 0$ — IVBAT(3)			105	µA
Dropout voltage(4): $VDO_{VRUSB3V1}$ (On mode)	$VDO_{VRUSB3V1} = VIN_{VRUSB3V1} – V_{VRUSB3V1}$ $I_{VRUSB3V1max} = 14$ mA — VBAT / USBIN			150	mV
Transient load regulation(5) (On mode)	$I_{VRUSB3V1min} \rightarrow I_{VRUSB3V1max}$ Slew 14 mA/15 ns			100	mV
Transient line regulation (On mode)	$VIN_{VRUSB3V1}$ drops 500 mV Slew: 40 mV/µs			20	mV
Wake-up time	Time required for the LDO to be ready for full load after sleep to active transition (during this time, load should be kept inside rated defined for sleep mode)			10	µs

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) IVBAT is the current sunk on the LDO VBAT.USB pin itself.
(4) For nominal output voltage
(5) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

Table 6-17. VUSB3V1 Internal LDO Regulator Characteristics(1) (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply recovery time	Time required for the LDO to return into specified output voltage range after switching from power source, that is, VBAT / VBUS / USBIN (during this time, USB module performance can be degraded).			150	µs
Overshoot	softstart			3%	
Pulldown resistance	Default in off mode	250	320	450	Ω

6.1.17 VUSB1V8 Regulator

The VUSB1V8 internal LDO regulator powers the USB subchip inside the TPS65951. Table 6-18 describes the regulator characteristics.

Table 6-18. VUSB1V8 Internal LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected between VINTUSB1P8.OUT and GND	0.5	2.2	2.7	µF
	Filtering capacitor ESR		0	10	600	mΩ
ELECTRICAL CHARACTERISTICS						
$VIN_{VUSB1V8}$	Input voltage	On mode: $VIN_{VUSB1V8}$= VBAT	2.7	3.6	4.5	V
$V_{VUSB1V8}$ (2)	Output voltage	$VIN_{VUSB1V8min}$ – $VIN_{VUSB1V8max}$	1.7	1.81	1.92	V
$I_{VUSB1V8}$	Rated output current	On mode			30	mA
	DC load regulation	$V_{VUSB1V8max}$ – $V_{VUSB1V8min}$ 0 < $I_{VUSB1V8}$ < 30 mA			20	mV
	DC line regulation	$V_{VUSB1V8min}$ – $V_{VUSB1V8max}$, $I_{VUSB1V8max}$			3	mV
	Turn-on time	$I_{VUSB1V8min}$ = 0, $C_{VUSB1V8}$ = 1 µF $V_{VUSB1V8}$ = $V_{VUSB1V8final}$ ±1%			100	µs
	Turn-off time	$I_{VUSB1V8max}$ = 30 mA, $C_{VUSB1V8}$ = 2.7 µF			5	ms
	Ripple rejection	$I_{VUSB1V8max}$ = 30 mA, $V_{INVUSB1V8}$ = $V_{VUSB1V8min}$ f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz	 50 40 30			dB
	Ground current	Off, $I_{VUSB1V8}$ = 0, 125°C On mode, $I_{VUSB1V8}$ = 0			3.5 90	µA
$VDO_{VUSB1V8}$	Dropout voltage(3)	$VDO_{VUSB1V8}$ = $VIN_{VUSB1V8}$ – $V_{VUSB1V8}$ $I_{VUSB1V8}$ = 15 mA			250	mV
	Transient load regulation(4)	$I_{VUSB1V8}$ = 5 mA → $I_{VUSB1V8}$ = 25 mA Slew 20 mA/2 ns			40	mV
	Transient line regulation	VIN_{VRUSB_1V8} drops 500 mV Slew: 40 mV/µs			20	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.18 VUSB1V5 Regulator

The VUSB1V5 internal LDO regulator powers the USB subchip inside the TPS65951. Table 6-19 describes the regulator characteristics.

Table 6-19. VUSB1V5 Internal LDO Regulator Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected between VINTUSB1P5 and GND	0.5	2.2	2.7	μF
	Filtering capacitor ESR		0	10	600	mΩ
ELECTRICAL CHARACTERISTICS						
$VIN_{VUSB1V5}$	Input voltage	On mode: $VIN_{VUSB1V5}$ = VBAT	2.7	3.6	4.5	V
$V_{VUSB1V5}$ (2)	Output voltage	$VIN_{VUSB1V5min}$ – $VIN_{VUSB1V5max}$	1.45	1.525	1.6	V
$I_{VUSB1V5}$	Rated output current	On mode			30	mA
	DC load regulation	$V_{VUSB1V5max}$ – $V_{VUSB1V5min}$ 0 < $I_{VUSB1V5}$ < 30 mA			20	mV
	DC line regulation	$V_{VUSB1V5min}$ – $V_{VUSB1V5max}$ $I_{VUSB1V5max}$			3	mV
	Turn-on time	$I_{VUSB1V5min}$ = 0, $C_{VUSB1V5}$ = 1 μF $V_{VUSB1V5}$ = $V_{VUSB1V5final}$ ±1%			100	μs
	Turn-off time	$I_{VUSB1V5max}$ = 30 mA, $C_{VUSB1V5}$ = 2.7 μF			5	ms
	Ripple rejection	$I_{VUSB1V5max}$ = 30 mA, $VIN_{VUSB1V5}$ = $V_{VUSB1V5min}$ f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz	50 40 30			dB
	Ground current	OFF, $I_{VUSB1V5}$ = 0, 125°C On mode, $I_{VUSB1V5}$ = 0			3.5 90	μA
$VDO_{VUSB1V5}$	Dropout voltage(3)	$VDO_{VUSB1V5}$ = $VIN_{VUSB1V5}$ – $V_{VUSB1V5}$ $I_{VUSB1V5}$ = 15 mA			250	mV
	Transient load regulation(4)	$I_{VUSB1V5}$ = 5 mA → $I_{VUSB1V5}$ = 25 mA Slew 20 mA/2 ns			40	mV
	Transient line regulation	$VIN_{VUSB1V5}$ drops 500 mV Slew: 40 mV/μs			20	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For the LDO characteristics to be fulfilled, a minimum of 250 mV between the LDO input and LDO output voltages is required.
(2) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(3) For nominal output voltage
(4) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.1.19 Charge Pump

The charge pump generates a 5.0-V (nominal) power supply voltage from the battery to the VBUS VUSBIN.CPOUT pin. The input voltage range is from 2.7 to 4.5 V for the battery voltage. The charge pump operating frequency is 1 MHz.

The charge pump tolerates 6 V on VUSBIN when it is in power-down mode. The charge pump integrates a short-circuit current limitation at 450 mA.

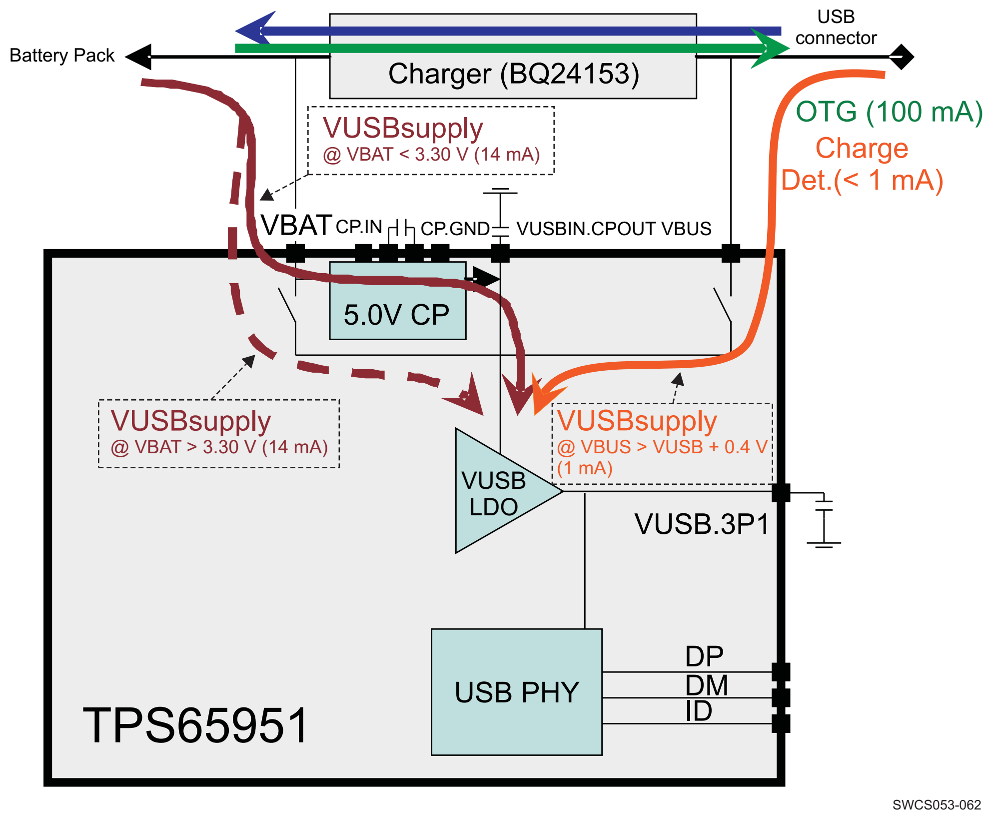


Figure 6-12. General Overview of the Charge Pump and its Interfaces

It can supply USB 3.1-V LDO when battery voltage is lower than this LDO VBATmin voltage (see Figure 6-11). By adding an external series switch under software control, the charge pump output voltage can be used as OTG supply in order to power OTG-B devices.

Table 6-20. Charge Pump Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor (1)	Connected between VUSBin.CPOUT and VSSP	1.41	4.7	6.5	μF
	Flying capacitor (1)	Connected between CP.CAPP and CP.CAPM	1.32	2.2	3.08	μF
	Filtering capacitor ESR				20	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage	On mode: V_{IN} = VBAT	2.7	3.6	4.5	V
V_O	Output voltage		4.625	5.0	5.25	V
I_{load}	Rated output current	VBAT > 3 V at VBUS	0		100	mA
		2.7 V < VBAT < 3 V, at VBUS	0		50	
	Efficiency	I_{LOAD} = 100 mA, VBAT = 3.6 V		55%		
	Setting time	$I_{LOADmax/2}$ to $I_{LOADmax}$ in 5 μs		100	400	μs
	Start-up time				3	ms
	Short-circuit limitation current		200	350	450	mA
	DC load regulation	$I_{LOADmin}$ to $I_{LOADmax}$		250	500	mV
	DC line regulation	3.0 V to $VBAT_{max}$ I_{LOAD} = 100 mA		250	500	mV
	Transient load regulation	$I_{VBUS_5Vmax/2}$ – I_{VBUS_5Vmax} 50 μs, C = 2 × 4.7 μF		300	350	mV
		0 – $I_{VBUS_5Vmax/2}$, 50 μs, C = 2 × 4.7 μF			350	
	Transient line regulation	$VBAT_{min}$ to $VBAT_{max}$ in 50 μs, C = 2 × 4.7 μF		300	350	mV

(1) The minimum filtering and flying capacitor values can be reduced to 1.2 μF, provided the charge pump is only used to supply VUSB3V1 LDO.

6.1.20 USB LDOs Short-Circuit Protection Scheme

The short-circuit current for the LDOs and DC-DCs in the TPS65951 is approximately twice the maximum load current. In certain cases when the output of the block is shorted to ground, the power dissipation can exceed the 1.2-W requirement if no action is taken. A short-circuit protection scheme is included in the TPS65951 to ensure that if the output of an LDO or DC-DC is short-circuited, then the power dissipation does not exceed the 1.2-W level.

The three USB LDOs VUSB3V1, VUSB1V8, and VUSB1V5 are included in this short-circuit protection scheme which monitors the LDO output voltage at a frequency of 1.6 Hz, and generates an interrupt (sc_it) when a short-circuit is detected.

The scheme compares the LDO output voltage to a reference voltage and detects a short-circuit if the LDO voltage drops below this reference value (0.5 or 0.75 V programmable). In the case of the VUSB3V1 and VUSB1V8 LDOs, the reference is compared with a divided down voltage (1.5 V typical).

If a short-circuit is detected on VRUSB3V1, then the power subchip FSM switches this LDO to sleep-mode.

If a short-circuit is detected on either VUSB1V8 or VUSB1V5, then the power subchip FSM switches the relevant LDO off.

6.1.21 RC Oscillators

Each DCDC has an integrated RC oscillator, which all have the same electrical characteristics (see Table 6-21). The usage of these RC oscillators is configurable through register bits, and by default the RC Oscillator of VDD1 is used for all DCDCs.

Table 6-21. RC Oscillator Characteristics

PARAMETERS	COMMENTS	MIN	TYP	MAX	UNIT
Input voltage range		1.425	1.5	1.575	V
Current consumption				55	μA
Internal frequency	After trim	2.25	3.2	3.75	MHz
Settling time				1	ms

6.2 Power References

The bandgap voltage reference is filtered (RC filter), using an external capacitor connected across the VREF output and an analog ground (REFGND). The VREF voltage is scaled, distributed, and buffered inside the device. The bandgap is started in fast mode (not filtered) and is set automatically by the power state machine in slow mode (filtered, less noisy) after switch on.

Table 6-22 describes the voltage reference characteristics.

Table 6-22. Voltage Reference Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITION						
	Filtering capacitor	Connected from V_{REF} to GNDREF	0.9	1	1.1	μF
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage	On mode	2.7	3.6	4.5	V
	Internal bandgap reference voltage	On mode, measured through TESTV terminal	1.203	1.215	1.227	V
	Reference voltage (V_{REF} terminal)	On mode	0.7425	0.75	0.7575	V
	Retention mode reference	On mode	0.492	0.5	0.508	V
	I_{REF} NMOS sink		0.9	1	1.1	μA
	Ground current	Bandgap I_{REF} block Preregulator V_{REF} buffer Retention reference buffer			25 20 15 10 10	μA
	Output spot noise	100 Hz			1	μV/√Hz
	A-weighted noise (rms)			200		nV (rms)
	P-weighted noise (rms)			150		nV (rms)
	Integrated noise	20 Hz to 100 kHz		2.2		μV
	I_{BIAS} trim bit LSB				0.1	μA
	Ripple rejection	< 1 MHz from VBAT	60			dB
	Start-up time				1	ms

6.3 Power Control

6.3.1 Backup Battery Charger

If the backup battery is rechargeable, then it can be recharged from the main battery. A programmable voltage regulator powered by the main battery allows recharging of the backup battery. The backup battery charge must be enabled using a control bit register. Charging starts when the following two conditions are met:

- Main battery voltage > backup battery voltage
- Main battery > VMBCH (see Table 6-24 for values)

Charging continues as long as the above listed conditions are met. Thereby there is a dead zone for BKBAT charging when the device is in ACTIVE state (occurs when VMBLO (2.7V typ) < VBAT < VMBCH (3.3V typ, programmable)).

The comparators of the BBS give the two thresholds of the backup battery charge start-up. The programmed voltage for the charger gives the end-of-charge threshold. The programmed current for the charger gives the charging current.

Overcharging is prevented by measurement of the backup battery voltage via the GPADC. Table 6-23 describes the backup battery charger characteristics.

Table 6-23. Backup Battery Charger Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBACKUP to MADC input attenuation	VBACKUP from 1.8 V to 3.3 V		0.33		V/V
Backup battery charging current	VBACKUP = 2.8 V, BBCHEN = 1, BBISEL = 00	10	25	45	µA
	VBACKUP = 2.8 V, BBCHEN = 1, BBISEL = 01	105	150	270	µA
	VBACKUP = 2.8 V, BBCHEN = 1, BBISEL = 10	350	500	900	µA
	VBACKUP = 2.8 V, BBCHEN = 1, BBISEL = 11	0.7	1	1.8	mA
	VBACKUP = 0 V, BBCHEN = 1, BBISEL = 00	17.5	25	45	µA
	VBACKUP = 0 V, BBCHEN = 1, BBISEL = 01	105	150	270	µA
	VBACKUP = 0 V, BBCHEN = 1, BBISEL = 10	350	500	900	µA
	VBACKUP = 0 V, BBCHEN = 1, BBISEL = 11	0.7	1	1.8	mA
End backup battery charging voltage: VBBCHGEND	$I_{VBACKUP}$ = –10 µA, BBSEL = 00	2.4	2.5	2.6	V
	$I_{VBACKUP}$ = –10 µA, BBSEL = 01	2.9	3.0	3.1	V
	$I_{VBACKUP}$ = –10 µA, BBSEL = 10	3.0	3.1	3.2	V
	$I_{VBACKUP}$ = –10 µA, BBSEL = 11	3.1	3.2	3.3	V

6.3.2 Battery Monitoring and Threshold Detection

6.3.2.1 Switch On/Switch Off and BACKUP Conditions

Table 6-24 summarizes the battery threshold levels.

Table 6-24. Battery Threshold Levels

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Main battery charged threshold VMBCH	Measured on VBAT terminal, VMBCH_SEL = 01	3.05	3.1	3.15	V
Main battery low threshold VMBLO	VBACKUP = 3.2 V, measured on VBAT terminal (monitored on terminal ONNOFF)	2.55	2.7	2.8	V
Main battery high threshold VMBHI	Measured on terminal VBAT, VBACKUP = 0 V Measured on terminal VBAT, VBACKUP = 3.2 V	2.5 2.5	2.65 2.85	3.0 3.0	V
Batteries not present threshold VBNPR	Measured on terminal VBACKUP or VBAT Measured on terminal VBAT with VBACKUP = 0 V, in slave mode	1.6 1.95	1.8 2.1	2.0 2.25	V

6.3.3 VRRTC LDO Regulator

The VRRTC voltage regulator is a programmable, low dropout, linear voltage regulator supplying (1.5 V typical) the embedded real-time clock (32.768-kHz oscillator) and dedicated I/Os of the digital host counterpart. The VRRTC regulator is also the supply voltage of the power-management digital state machine. The VBRTC regulator is supplied from the uninterrupted power rail (UPR) line, which is connected to the main battery through a clamp circuit or to the backup battery, depending on the battery states. The VRRTC output is present as long as a valid energy source is present. The VRTC.OUT pin is supplied by the VRRTC LDO when VBAT rises above VMBHI (= 2.85 V typical), and by the VBRTC circuit when VBAT falls below VMBLO (= 2.7 V typical).

Table 6-25 describes the regulator characteristics.

Table 6-25. VRRTC LDO Regulator Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS						
	Filtering capacitor	Connected from VRTC.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS						
V_{IN}	Input voltage	On mode	2.7	VBAT	4.5	V
V_{OUT} (1)	Output voltage		1.45	1.5	1.55	V
I_{OUT}	Rated output current	On mode			30	mA
		Sleep mode			5	
	DC load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			100	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			100	mV
	Turn-on time	$I_{OUT} = 0$, at $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		μs
	Wake-up time	On mode from low power to On mode, $I_{OUT} = 0$, at $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		μs
		From backup to on mode, $I_{OUT} = 0$, at $V_{OUT} = V_{OUTfinal} \pm$ 3%		100		
	Ripple rejection (VRRTC)	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	50 40 30			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 1$ mA Off mode			70 100 10 11 1	μA
V_{DO}	Dropout voltage (2)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation (3)	I_{LOAD}: $I_{MIN} - I_{MAX}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV
	Overshoot	softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(2) For nominal output voltage
(3) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, then follow the output voltage specification.

6.3.4 VBRTC Clamp

Table 6-26 describes the clamp characteristics.

Table 6-26. VBRTC Clamp Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT LOAD CONDITIONS					
Filtering capacitor	Connected from VRTC to analog ground	0.3	1	2.7	μF
Filtering capacitor ESR		20		600	mΩ
ELECTRICAL CHARACTERISTICS					
Input voltage V_{IN}	Active Backup mode, VBAT < 1.8 V	1.8 VBNPRmin		3.3 VBBCHENDmax	V
Output voltage V_{OUT}	Backup mode	1.0	1.3	1.55	V
Rated output current I_{OUT}	Backup mode			100	μA
DC load regulation	Backup mode, $I_{OU\ T}$ = I_{OUTmax} to 0			100	mV
Turn-on time	I_{OUT} = 0, at V_{OUT} = $V_{OUTfinal}$ ±3%		1		ms
Ground current	Backup mode, at 27°C, V_{IN} = 3.0 V		0.5		μA

6.3.5 Hot-Die Detection and Thermal Shutdown

6.3.5.1 Hot-Die Characteristics

The hot-die threshold value is selected with the MSC_CFG[7:6]TEMP_SEL register bits.

Table 6-27. Thermal Hot-Die Selection

MSC_CFG[7:6]TEMP_SEL	Threshold (nominal)(1)
00 (1st Hot-Die threshold)	Rising temp: 120°
	Falling temp: 111°
01 (2nd Hot-Die threshold)	Rising temp: 130°
	Falling temp: 121°
10 (3rd Hot-Die threshold)	Rising temp: 140°
	Falling temp: 131°
11 (4th Hot-Die threshold)	Not used

(1) The min/max range is ±5%

6.3.5.2 Thermal Shutdown Characteristics

Table 6-28. Thermal Enable Selection

Thermal Shutdown	Threshold (nominal)(1)
Enable	Rising temp: 150°
	Falling temp: 140°

(1) The min/max range is ±5%

6.3.5.3 Thermal Detect System Consumption

Table 6-29. Thermal Detect System Consumption

Parameter	Conditions	Min	Typ	Max	Units
Thermal shutdown detector consumption	System enable (hardware or software)	40	55	70	µA
Hot-die detector consumption			3	5	µA

6.4 Power Consumption

Table 6-30 describes the power consumption depending on the use cases.

NOTE

The typical power consumption is obtained in the nominal operating conditions and with the TPS65951 standalone.

Table 6-30. Power Consumption (for C027 and C021/C014 Boot Modes)

MODE	STATE	DESCRIPTION	VBAT	CONSUMPTION	
				TYPICAL	MAX
C027 Boot mode	BACKUP	Only the RTC date is maintained with a couple of registers in the backup domain. No main source is connected. The consumption is on the backup battery.	not present	2.25 µA × 3.2 V = 7.2 µW	
	WAIT-ON	The phone is apparently off for the user, a main battery is present and well charged. The RTC registers, registers in backup domain are maintained. The wakeup capabilities (like the PWRON button) are available.	3.8 V	64 µA × 3.8 V = 243.2 µW	
	ACTIVE (No Load) HFCLK = 26 MHz	Subsystem is powered by the main battery, all supplies are enabled with no external load, internal reset is released and the associated processor is running.	3.8 V	3786 µA × 3.8 V = 14387 µW	
	SLEEP (No Load)	The main battery powers subsystem, selected supplies are enabled but in low-consumption mode and associated processor is in low-power mode.	3.8 V	558 µA × 3.8 V = 2120 µW	
C021/ C014 Boot mode	BACKUP	Only the RTC date is maintained with a couple of registers in the backup domain. No main source is connected. The consumption is on the backup battery.	not present	2.25 µA × 3.2 V = 7.2 µW	5 µA × 3.2 V = 16 µW
	WAIT-ON	The phone is apparently off for the user, a main battery is present and well charged. The RTC registers, registers in backup domain are maintained. The wakeup capabilities (like the PWRON button) are available.	3.8 V	64 µA × 3.8 V = 243.2 µW	100 µA × 3.8 V = 380 µW
	ACTIVE (No Load) HFCLK = 26 MHz	Subsystem is powered by the main battery, all supplies are enabled with no external load, internal reset is released and the associated processor is running.(1)	3.8 V	3490 µA × 3.8 V = 13262 µW	
	ACTIVE (No Load) HFCLK = 38.4 MHz			4374 µA × 3.8 V = 16621 µW	4000 µA × 3.8 V + 7000 µA × 1.8 V = 27800 µW
	SLEEP (No Load)	The main battery powers subsystem, selected supplies are enabled but in low-consumption mode and associated processor is in low-power mode.(1)	3.8 V	554 µA × 3.8 V = 2105 µW	800 µA × 3.8 V + 30 µA × 1.8 V = 3094 µW

(1) Typical value includes current consumption under VBAT + current consumption under VIO normalized.

Table 6-31 provides the different regulator states according to the used mode.

Table 6-31. Regulator States Depending on Use Cases

REGULATOR	MODE: C021/C014 (Master/Slave) and C027 (Master)			
	BACKUP	WAIT-ON	SLEEP (No Load)	ACTIVE (No Load)
VAUX1	OFF	OFF	OFF	OFF
VAUX2	OFF	OFF	OFF	OFF
VAUX3	OFF	OFF	OFF	OFF
VAUX4	OFF	OFF	OFF	OFF
VMMC1	OFF	OFF	OFF	OFF
VMMC2	OFF	OFF	OFF	OFF
VPLL1	OFF	OFF	SLEEP	ON
VPLL2	OFF	OFF	OFF	OFF
VDAC	OFF	OFF	OFF	OFF
VINTANA1	OFF	OFF	SLEEP	ON
VINTANA2	OFF	OFF	SLEEP	ON
VINTDIG	OFF	OFF	SLEEP	ON
VIO	OFF	OFF	SLEEP	ON
VDD1	OFF	OFF	SLEEP	ON
VDD2	OFF	OFF	SLEEP	ON
VUSB1V5	OFF	OFF	OFF	OFF
VUSB1V8	OFF	OFF	OFF	OFF
VUSB3V1	OFF	OFF	SLEEP	SLEEP

6.5 Power Management

6.5.1 Master/Slave Modes

- Master:
  TPS65951 decides to switch on or off the system and control the other power ICs in the system with the SYSEN output.
- Slave:
  TPS65951 is controlled by another power IC with a digital signal on the PWRON input. There is no battery management in slave mode.

6.5.2 Boot Modes

The modes corresponding to BOOT0–BOOT1 combination value are:

Table 6-32. BOOT Mode Description

NAME	DESCRIPTION	BOOT0	BOOT1
MC021/MC014[(1)]	Master_C021/CO14_Generic 10	1	0
SC021/SC014	Slave_C021/CO14_Generic 11	1	1

(1) Boot mode for OMAP34xx/OMAP36xx is MC021/MC014 boot mode.

6.5.3 Process Modes

This parameter defines:

- The boot voltage for the host core
- The boot sequence associated with the process
- The DVFS protocol associated with the process

6.5.3.1 C021/C014 Mode

Table 6-33. C021/CO14 Mode Description

Boot core voltage	1.2 V
Power sequence	VIO followed by VPLL1, VDD2, VDD1
DVFS protocol	SmartReflex IF (I^2C high speed)

6.5.4 Switch-On Sequence

6.5.4.1 Timings Before Sequence_Start

Sequence_Start is a symbolic internal signal to ease the description of the power sequences and occurs according to the different events detailed in Figure 6-13.

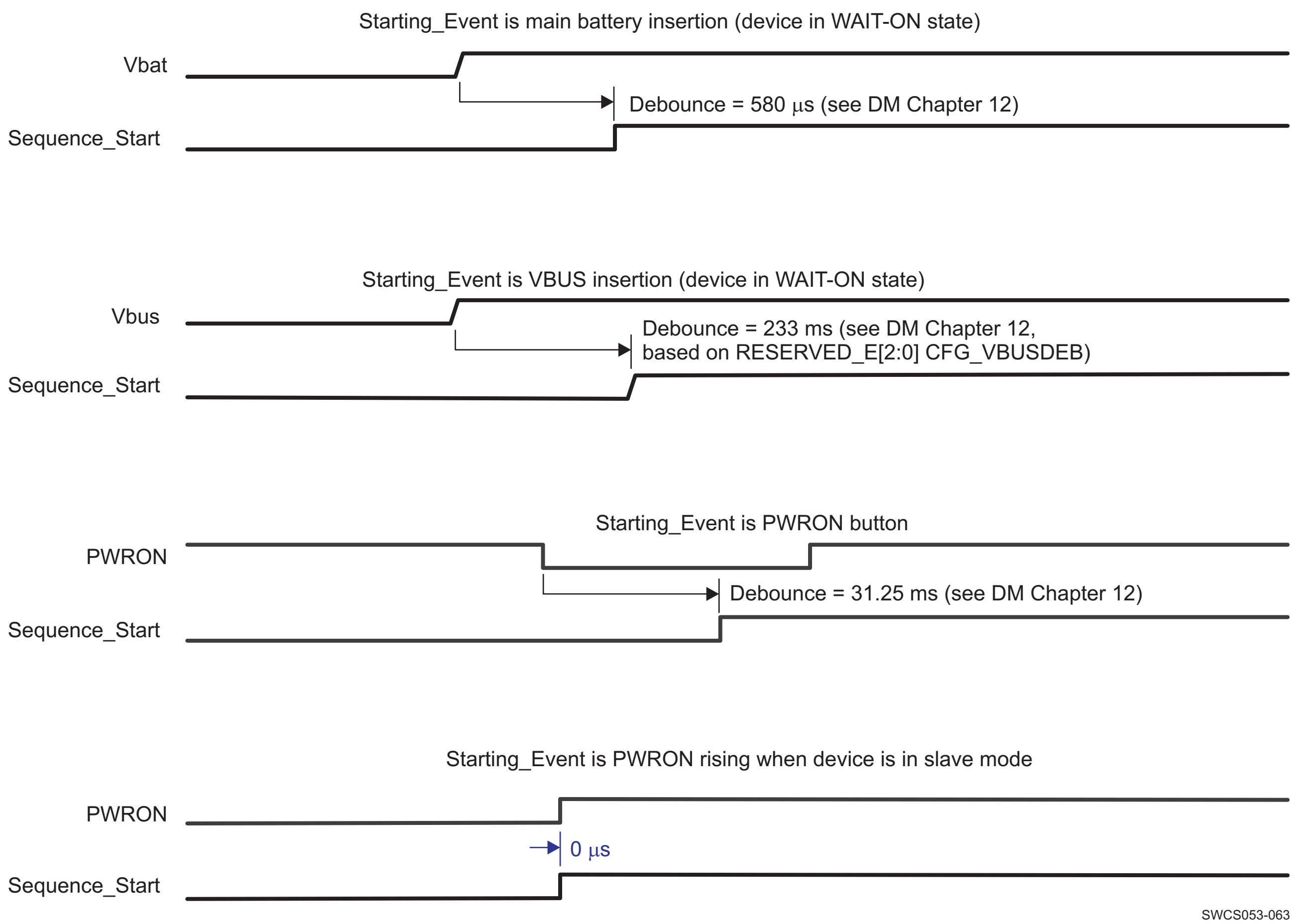


Figure 6-13. Timings Before Sequence Start

6.5.4.2 Switch On in Master_C021/C014_Generic Mode

Figure 6-14 describes the timing and control that must occur in the Master_C0271/CO14_Generic mode. Sequence_Start is a symbolic internal signal to ease the description of the power sequences and occurs according to the different events detailed in Figure 6-13.

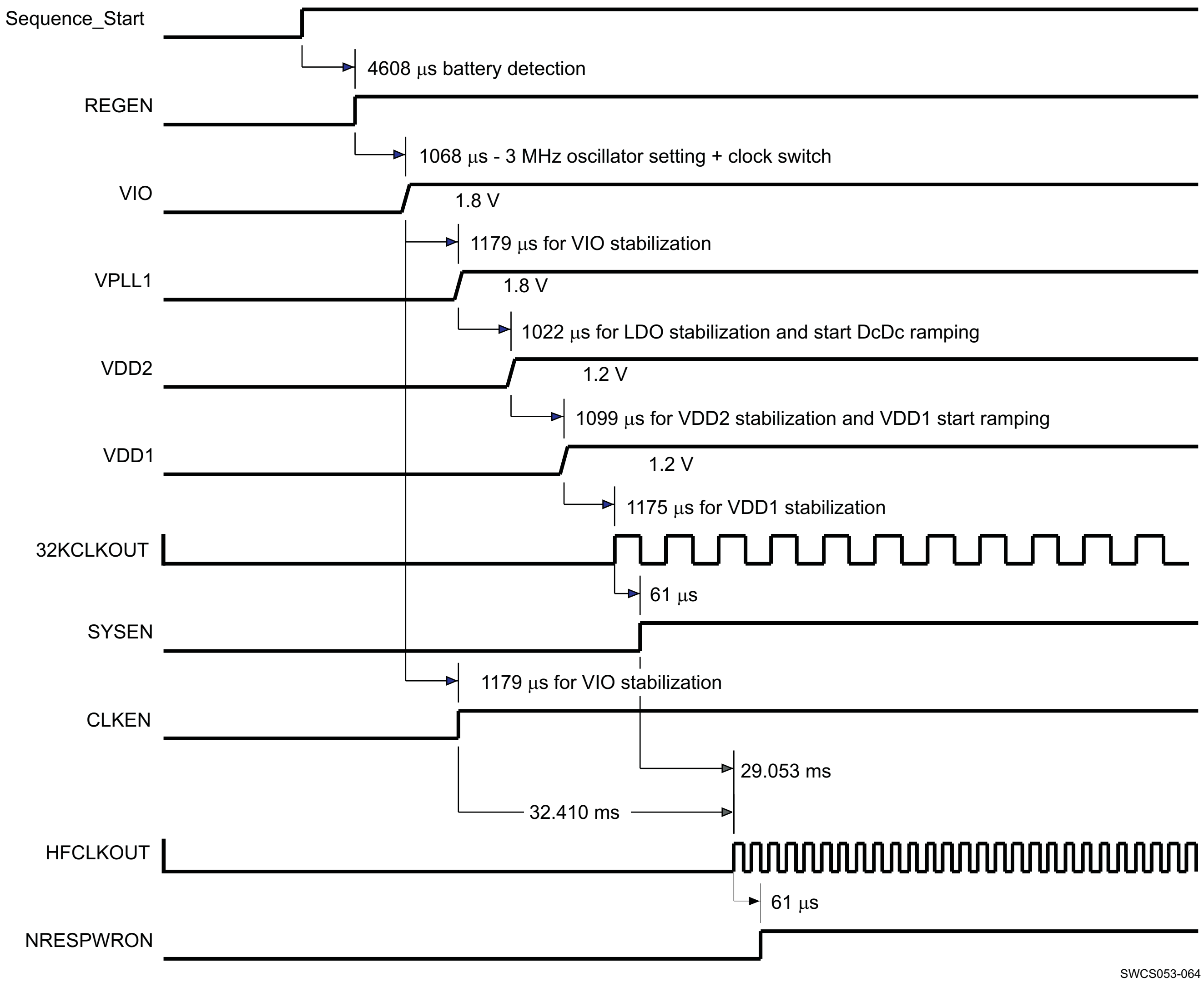
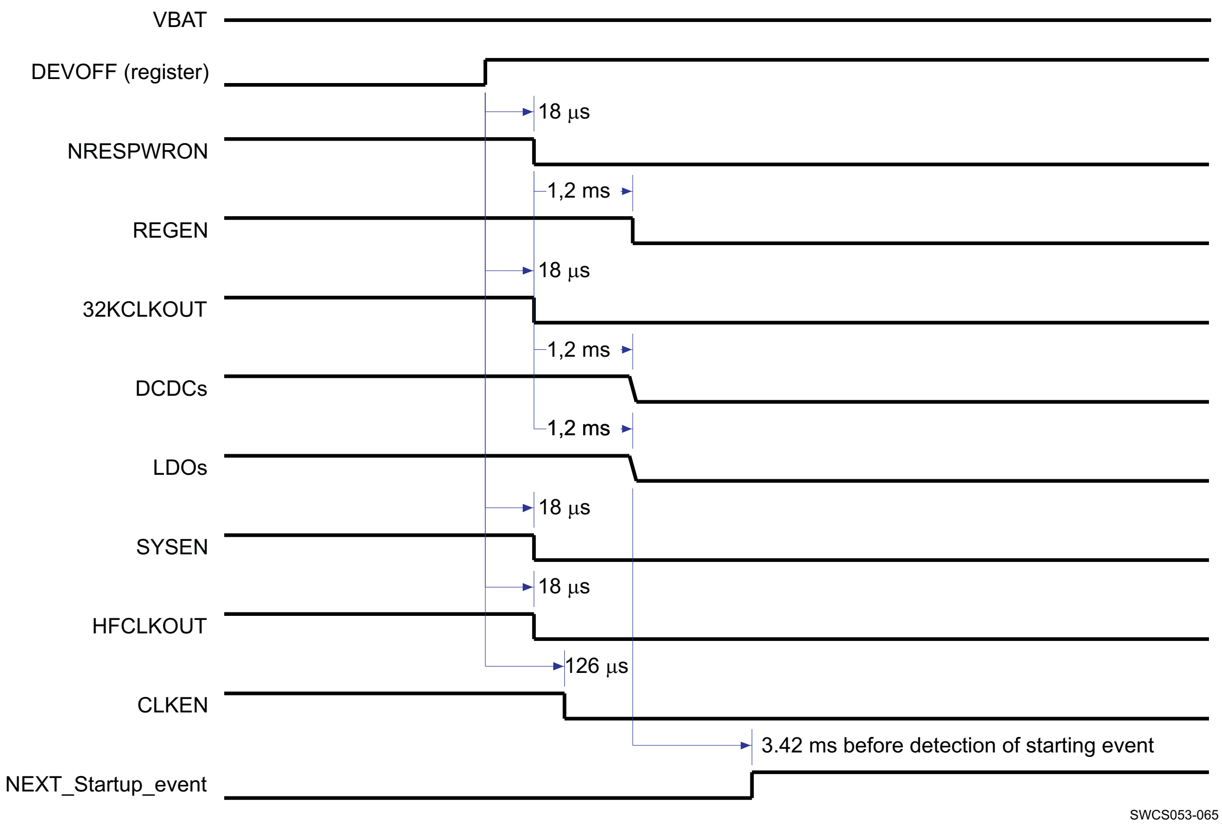


Figure 6-14. Timings—Switch On in Master_C021/C014_Generic Mode

6.5.5 Switch-Off Sequence

Figure 6-15 describes the timing and control that occur during the switch-off sequence in master modes.



NOTE: All of these timings are the typical values with the default setup (depending on the resynchronization between power domains, state machinery priority, etc.).

Figure 6-15. Switch-Off Sequence in Master Modes

The DEVOFF event is the only switch-off event that follows the hard-coded switch-off sequence. So, the switch-off sequence is valid only for a controlled switch off (DEVOFF). In case of a hardware switch-off event, all resources will be stopped at once.

In case the HF clock value is different from 19.2 MHz (with HFCLK_FREQ bit field values set accordingly inside the CFG_BOOT register), then the delay between DEVOFF and NRESPWRON/32KCLKOUT/SYSEN/HFCLKOUT is divided by two (meaning around 9 µs). This is due to the internal frequency used by POWER STM switching from 3.2 MHz to 1.6 MHz in case the HF clock value is 19.2 MHz.

The DEVOFF event is PWRON falling edge in slave mode and DEVOFF internal register write in master mode.

7 Connectivity

7.1 Timing Parameters

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated as shown in Table 7-1.

Table 7-1. Timing Parameters

SUBSCRIPTS	
SYMBOL	**PARAMETER**
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
H	High
L	Low
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

7.2 Target Frequencies

Table 7-2 assumes testing over the recommended operating conditions.

Table 7-2. TPS65951 Interface Target Frequencies

I/O INTERFACE	INTERFACE DESIGNATION		TARGET FREQUENCY 1.5 V
SmartReflex I^{2}C[1] General-purpose I^{2}C	Inter-Integrated Circuit Interface	Slave high-speed mode for HFCLKIN = 19.2 MHz	2.2 Mbps
		Slave high-speed mode for HFCLKIN = 26 MHz	2.4 Mbps
		Slave high-speed mode for HFCLKIN = 38.4 MHz	2.9 Mbps
		Slave fast-speed standard mode	400 kbps
		Slave standard mode	100 kbps
USB	Universal serial bus	High speed	480 Mbps
		Full speed	12 Mbps
		Low speed	1.5 Mbps
JTAG	Joint Test Action Group, IEEE 1149.1 standard		30 MHz
TDM/I2S	I2S		1/(64 × Fs)[2]
	Right justified		1/(64 × Fs)[2]
	Left justified		1/(64 × Fs)[2]
	TDM		1/(128 × Fs)[2]
Voice Interface	Pulse code modulation		1/(65 × Fs)[3]

(1) There is no limitation for I2C SmartReflex communication with OMAP.
(2) Fs = 8 kHz to 48 kHz; 96 kHz for RX path only (TDM/I2S interface)
(3) Fs = 8 kHz or 16 kHz (voice interface)

7.3 USB Transceiver

The TPS65951 device includes a universal serial bus (USB) on-the-go (OTG) transceiver that supports USB 480 Mbps high-speed (HS), 12 Mbps full-speed (FS), and USB 1.5 Mbps low-speed (LS) through a 4-pin UTMI+ low pin interface (ULPI).

It also includes a module covering Battery Charging Specification v1.0.

Figure 7-1 shows the USB 2.0 PHY highlight block diagram.

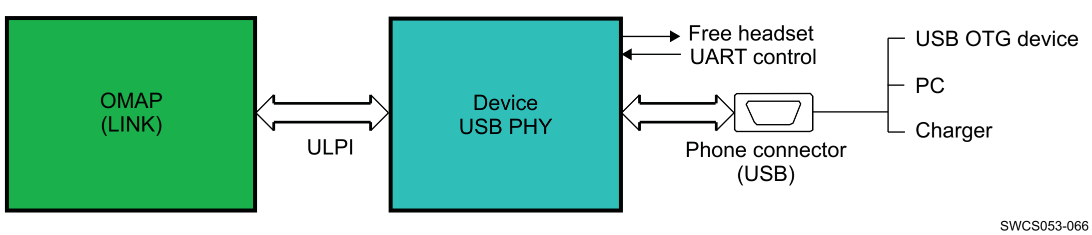


Figure 7-1. USB 2.0 PHY Highlight

Figure 7-2 shows the USB system application schematic.

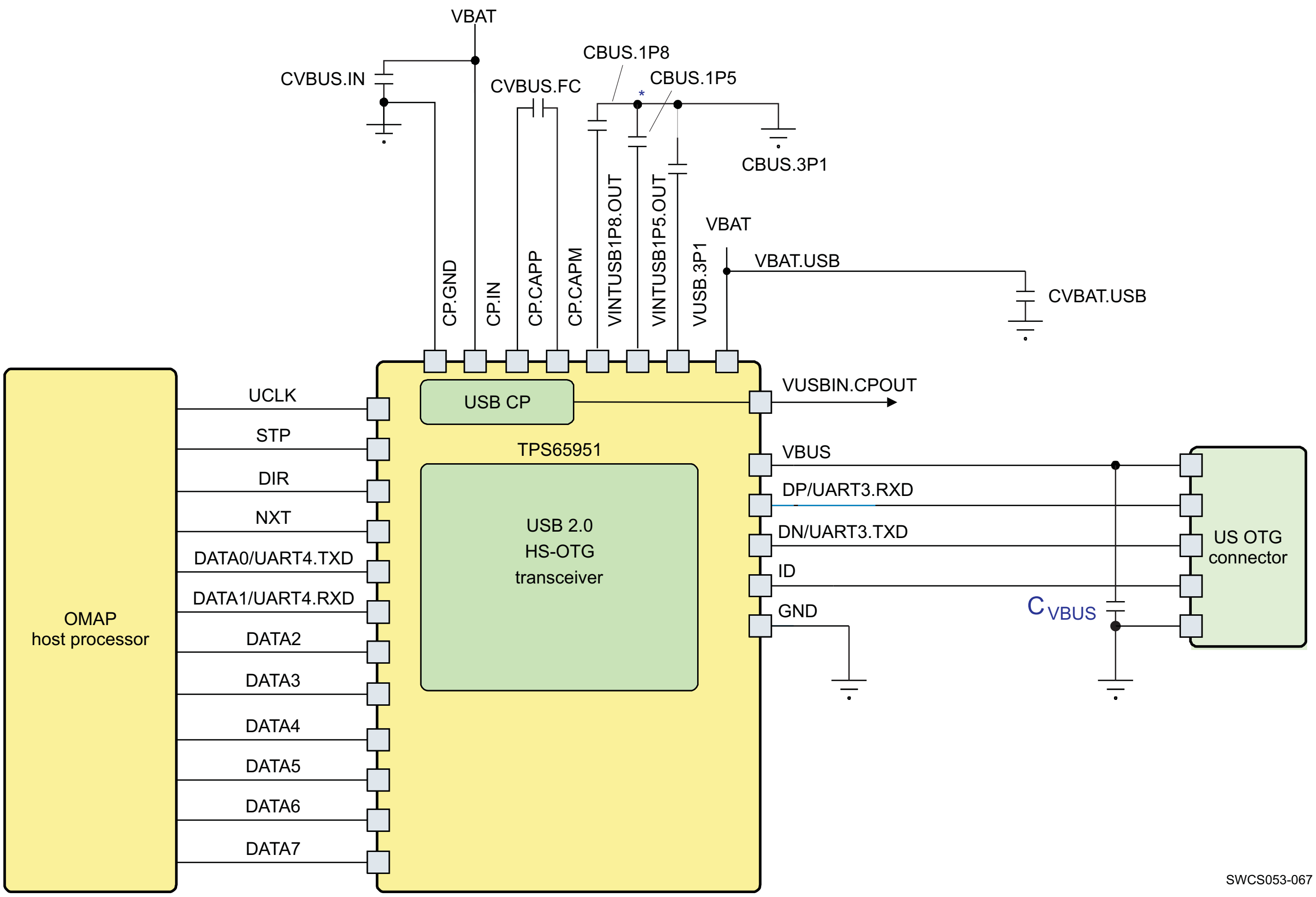


Figure 7-2. USB System Application Schematic

NOTE

For the component values, see Table 12-1, *TPS65951 External Components*.

7.3.1 PHY Electrical Characteristics

The PHY is the physical signaling layer of the USB 2.0. It essentially contains all the drivers and receivers needed for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through ULPI.

The transmitters and receivers inside the PHY are classified into two main classes:

- The full-speed (FS) and low-speed (LS) transceivers. These are the legacy USB1.x transceivers.
- The high-speed (HS) transceivers

In order to bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A DPLL which does a frequency multiplication to achieve the 480-MHz low-jitter lock necessary for USB and also the clock required for the switched capacitor resistance block.
- A switched capacitor resistance block which is used to replicate an external resistor on chip.

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

Apart from this, the PHY also contains circuitry which protects it from accidental 5-V short on the DP and DM lines.

7.3.1.1 LS/FS Single-Ended Receivers

In addition to the differential receiver, there is a single-ended receiver (SE–, SE+) for each of the two data lines D+/–. The main purpose of the single-ended receivers is to qualify the D+ and D– signals in the full-speed/low-speed modes of operation.

Table 7-3. LS/FS Single-Ended Receivers

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
USB Single-Ended Receivers						
Skew between VP and VM	SKWVP_VM	Driver outputs unloaded	–2	0	2	ns
Single-ended hysteresis	V_{SE_HYS}		50			mV
High (driven)	V_{IH}		2			V
Low	V_{IL}				0.8	V
Switching threshold	V_{TH}		0.8		2	V

7.3.1.2 LS/FS Differential Receiver

A differential input receiver (RX) retrieves the LS/FS differential data signaling. The differential voltage on the line is converted into digital data by a differential comparator on DP/DM. This data is then sent to a clock and data recovery circuit which recovers the clock from the data. An additional serial mode exists in which the differential data is directly output on the RXRCV pin.

Table 7-4. LS/FS Differential Receiver

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
Differential input sensitivity	V_{DI}	Ref. USB2.0	200			mV
Differential common mode range	V_{CM}	Ref. USB2.0	0.8		2.5	V

7.3.1.3 LS/FS Transmitter

The USB transceiver (TX) uses a differential output driver to drive the USB data signal D+/– onto the USB cable. The driver's outputs support 3-state operation to achieve bidirectional half-duplex transactions.

Table 7-5. LS Transmitter

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
Low	V_{OL}	Ref. USB2.0	0		300	mV
High (driven)	V_{OH}	Ref. USB2.0	2.8		3.6	V
Output signal crossover voltage	Vcrs	Ref. USB2.0, covered by eye diagram	1.3		2	V
Rise time	t_{Fr}	Ref. USB2.0, covered by eye diagram	75		300	ns
Fall time	t_{Ff}		75		300	ns
Differential Rise and Fall Time Matching	TFRFM		80%		125%	
Low-speed Data Rate	TFDRATE		1.4775		1.5225	Mbps
Source jitter Total (including frequency tolerance): - To Next Transition - For Paired Transitions	 TDJ1 TDJ2	Ref. USB2.0, covered by eye diagram	 –25 –10		 25 10	ns
Source SE0 interval of EOP	TFEOPT	Ref. USB2.0, covered by eye diagram	1.25		1.5	µs
Downstream eye diagram		Ref. USB2.0, covered by eye diagram				
Differential Common Mode Range	V_{CM}	Ref. USB2.0	0.8		2.5	V

Table 7-6. FS Transmitter

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
Low	V_{OL}	Ref. USB2.0	0		300	mV
High (driven)	V_{OH}	Ref. USB2.0	2.8		3.6	V
Output signal crossover voltage	Vcrs	Ref. USB2.0, covered by eye diagram	1.3		2	V
Rise time	t_{Fr}	Ref. USB2.0	4		20	ns
Fall time	t_{Ff}		4		20	ns
Differential Rise and Fall Time Matching	TFRFM		90%		111.11 %	
Driver output resistance	ZDRV	Ref. USB2.0	28		44	Ω
Full-speed Data Rate	TFDRATE	Ref. USB2.0, covered by eye diagram	11.97		12.03	Mbps
Source jitter Total (including frequency tolerance):						
- To Next Transition	TDJ1	Ref. USB2.0, covered by eye diagram	–2		2	ns
- For Paired Transitions	TDJ2		–1		1	
Source SE0 interval of EOP	TFEOPT	Ref. USB2.0, covered by eye diagram	160		175	ns
Downstream eye diagram		Ref. USB2.0, covered by eye diagram				
Upstream eye diagram						

7.3.1.4 HS Differential Receiver

The high-speed receiver consists of the following blocks:

- A differential input comparator to receive the serial data
- A squelch detector to qualify the received data
- An oversampler-based clock data recovery scheme followed by a NRZI decoder, bit unstuffing, and serial-to-parallel converter to generate the UTMI DATAOUT

Table 7-7. HS Differential Receiver

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
High-speed squelch detection threshold (differential signal amplitude)	V_{HSSQ}	Ref. USB2.0	100		150	mV
High-speed disconnect detection threshold (differential signal amplitude)	V_{HSDSC}	Ref. USB2.0	525		625	mV
High-speed differential input signaling levels		Ref. USB2.0, specified by eye pattern templates				mV
High-speed data signaling common mode voltage range (guidelines for receiver)	V_{HSCM}	Ref. USB2.0	–50		500 (1)	mV
Receiver jitter tolerance		Ref. USB2.0, specified by eye pattern templates			150	ps

(1) For low-frequency chirp signaling, the max common mode voltage range value is 600 mV.

7.3.1.5 HS Differential Transmitter

The high-speed transmitter is always operated on the UTMI parallel interface. The parallel data on the interface is serialized, bit stuffed, NRZI encoded, and transmitted as a dc output current on DP or DM depending on the data. Each line has an effective 22.5-Ω load to ground, which generates the voltage levels for signaling.

A disconnect detector is also part of the HS transmitter. A disconnect on the far end of the cable causes the impedance seen by the transmitter to double thereby doubling the differential amplitude seen on the DP/DM lines.

Table 7-8. HS Transmitter

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
High-speed idle level	V_{HSOI}	Ref. USB2.0	–10		10	mV
High-speed data signaling high	V_{HSOH}	Ref. USB2.0	360		440	mV
High-speed data signaling low	V_{HSOL}	Ref. USB2.0	–10		10	mV
Chirp J level (differential voltage)	V_{CHIRPJ}	Ref. USB2.0	700		1100	mV
Chirp K level (differential voltage)	V_{CHIRPK}	Ref. USB2.0	–750		–500	mV
Rise time (10% – 90%)	t_{HSR}	Ref. USB2.0, covered by eye diagram	500			ps
Fall time (10% – 90%)	t_{HSF}	Ref. USB2.0, covered by eye diagram	500			ps
Driver output resistance (which also serves as high-speed termination)	Z_{HSDRV}	Ref. USB2.0	40.5		49.5	Ω
High-speed data range	THSDRAT	Ref. USB2.0, covered by eye diagram	479.76		480.24	Mbps
Data source jitter		Ref. USB2.0, covered by eye diagram				
Downstream eye diagram		Ref. USB2.0, covered by eye diagram				
Upstream eye diagram		Ref. USB2.0, covered by eye diagram				

7.3.1.6 UART Transceiver

In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver.

Table 7-9. USB UART Interface Timing Parameters

PARAMTER		MIN	MAX	UNIT
$t_{PH_DP_CON}$	Phone D+ connect time	100		
$t_{PH_DISC_DET}$	Phone D+ disconnect time	150		
f_{UART_DFLT}	Default UART signaling rate (typical rate)		9600	bps

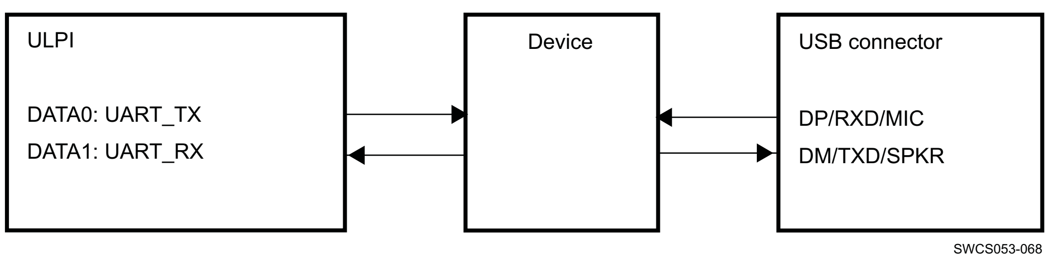


Figure 7-3. USB UART Data Flow

Table 7-10. CEA-2011/UART Interface Timing Parameters

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
UART Transmitter CEA-2011						
Phone UART edge rates	$t_{PH_UART_EDGE}$	DP_PULLDOWN asserted			1	µs
Serial interface output high	V_{OH_SER}	ISOURCE = 4 mA	2.4	3.3	3.6	V
Serial interface output low	V_{OL_SER}	ISINK = –4 mA	0	0.1	0.4	V
UART Receiver CEA-2011						
Serial interface input high	V_{IH_SER}	DP_PULLDOWN asserted	2			V
Serial interface input low	V_{IL_SER}	DP_PULLDOWN asserted			0.8	V
Switching threshold	V_{TH}		0.8		2	V

7.3.1.7 Pullup/Pulldown Resistors

Table 7-11. Pullup/Pulldown Resistors

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
Pullup Resistors						
Bus pullup resistor on upstream port (idle bus)	R_{PUI}	Bus idle	0.9	1.1	1.575	kΩ
Bus pullup resistor on upstream port (receiving)	R_{PUA}	Bus driven/driver's outputs unloaded	1.425	2.2	3.09	kΩ
High (floating)	V_{IHZ}	Pullups/pulldowns on both DP and DM lines	2.7		3.6	V
Phone D+ pullup voltage	$V_{PH_DP_UP}$	Driver's outputs unloaded	3	3.3	3.6	V
Pulldown Resistors						
Phone D+/– pulldown	$R_{PH_DP_DWN}$ $R_{PH_DM_DWN}$	Driver's outputs unloaded	14.25	18	24.8	kΩ
D+/– Data Line						
Upstream facing port	C_{INUB}	[1.0]		22	75	pF
On-the-go device leakage	$V_{OTG_DATA_LKG}$	[2]			0.342	V
Input impedance exclusive of pullup/pulldown	Z_{INP}	Driver's outputs unloaded	300			kΩ

7.3.2 OTG Electrical Characteristics

The on-the-go (OTG) block integrates three main functions:

- The USB plug detection function on VBUS and ID
- The ID resistor detection
- The VBUS level detection

7.3.2.1 OTG VBUS Electrical

Table 7-12. OTG VBUS Electrical

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
VBUS Wake-Up Comparator						
V_{BUS} wake-up delay	$DEL_{VBUS_WK_UP}$				15	μs
VBUS Comparators						
A-device session valid	$V_{A_SESS_VLD}$		0.8	1.4	2.0	V
Hysteresis for A-device session valid comparator			30	70	130	mV
A-device V_{BUS} valid	$V_{A_VBUS_VLD}$		4.4	4.5	4.625	V
B-device session end	$V_{B_SESS_END}$		0.2	0.5	0.8	V
B-device session valid	$V_{B_SESS_VLD}$		2.1	2.4	2.7	V
Hysteresis for B-device session valid comparator			50	110	250	mV
VBUS Line						
A-device V_{BUS} input impedance to ground (SRP (V_{BUS} pulsing) capable A-device not driving V_{BUS})	$R_{A_BUS_IN}$	For VBUS = 0 to 2.1 V	13.77		100	kΩ
		For VBUS = 2.1V to 5.25 V	2.1		100	
		For VBUS = 5.25 V	13.77		30	
B-device V_{BUS} SRP pulldown	$R_{B_SRP_DWN}$	5.25 V/8 mA, Pullup voltage = 3 V	5	10	20	kΩ
B-device V_{BUS} SRP pullup	$R_{B_SRP_UP}$	(5.25 V – 3 V)/8 mA, Pullup voltage = 3 V	0.85	1.3	1.75	kΩ
B-device V_{BUS} SRP rise time maximum for OTG-A communication	$t_{RISE_SRP_UP_MAX}$	0 to 2.1 V with < 13 μF load			34	ms
B-device V_{BUS} SRP rise time minimum for standard host connection	$t_{RISE_SRP_UP_MIN}$	0.8 to 2.0 V with > 97 μF load	46			ms
V_{BUS} leakage					10	μA

7.3.2.2 OTG ID Electrical

Table 7-13. OTG ID Electrical

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
ID Wake-Up Comparator						
ID wake-up comparator	$R_{ID_WK_UP}$	Wake-up when ID shorted to ground.	30		100	kΩ
ID Comparators — ID External Resistors Specifications						
ID ground comparator	R_{ID_GND}	ID_GND interrupt	4	20	25	kΩ
ID Float comparator	R_{ID_FLOAT}	ID_FLOAT interrupt	200		500	kΩ
ID Line						
Phone I_D pulldown	$R_{PH_ID_DWN}$		0.25		2	kΩ
Phone I_D pullup to $V_{PH_ID_UP}$	$R_{PH_ID_UP}$	ID unloaded VUSB3V1	70	90	286	kΩ
Phone I_D pullup voltage	$V_{PH_ID_UP}$	Connected to VUSB3V1	2.5		3.2	V
ID line maximum voltage					5.25	V

7.3.3 Charger Detection

In order to support Battery Charging Specification v1.1 [BCS v1.1], a charger detection module is included inside TPS65951 USB module.

The detection mechanism aims distinguishing several types of power sources that can be connected on VBUS line:

- Dedicated Charger Port
- Standard Host Port
- Charging Host Port

This includes:

- a dedicated voltage referenced pull-up on DP line
- a dedicated current controlled pull-down on DM line
- a detection comparator on DM line
- a control/detection state machine including timers
- a charger detection output pin (CHRG_DET_N) for external charger control

Additional circuitry is added on DP/DM respectively for data line symmetry (required for HS operation) and for possible future extension.

ID pin status detection (as defined per OTG v1.3 standard) and DP/DM Single-Ended receivers (as defined per USB v2.0 standard) are also used to determine the type of device plugged on USB connector.

For details on the detection mechanism, refer to [BCS v1.1].

7.4 Inter-Integrated Circuit (I^2C) Timing

The TPS65951 provides two I^2C high-speed slave interfaces (one for general-purpose and one for SmartReflex). These interfaces support the standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (2.2 Mbps for HFCLKIN = 19.2 MHz, 2.4 Mbps for HFCLKIN = 26 MHz and 2.9 Mbps for HFCLKIN = 38.4 MHz(1)). The general-purpose I^2C module embeds four different slave hard-coded addresses (ID1 = 48h, ID2 = 49h, ID3 = 4Ah, and ID4 = 4Bh). The SmartReflex I^2C module uses one slave hard-coded address (ID5). The master mode is not supported.

(1) There is no limitation for I^2C SmartReflex communication with OMAP.

Table 7-14 and Table 7-15 assume testing over the recommended operating conditions (see Figure 7-4).

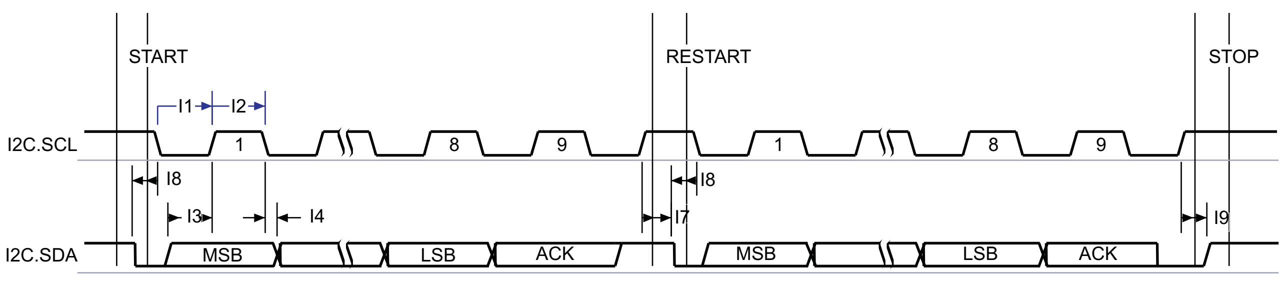


Figure 7-4. I^2C Interface—Transmit and Receive in Slave Mode

Table 7-14. I2C Interface Timing Requirements(1) (2)

NO.	PARAMETER			MIN	MAX	UNIT
Slave High-Speed Mode						
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high		10		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	at 2.2Mbps	0	180	ns
			at 2.4Mbps	0	155	ns
			at 2.9Mbps	0	100	ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	at 2.2Mbps	270		ns
			at 2.4Mbps	245		ns
			at 2.9Mbps	190		ns
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low		160		ns
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high		160		ns
Slave Fast-Speed Mode						
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high		100		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low		0	0.9	µs
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low		0.6		µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low		0.6		µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high		0.6		µs
Slave Standard Mode						
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high		250		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low		0		ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low		4.7		µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low		4		µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high		4		µs

(1) The input timing requirements are given by considering a rising or falling time of:
80 ns in high-speed mode (3.4 Mbps)
300 ns in fast-speed mode (400 kbps)
1000 ns in standard mode (100 kbps)
(2) SDA is equal to I2C.SR.SDA or I2C.CNTL.SDA
SCL is equal to I2C.SR.SCL or I2C.CNTL.SCL

Table 7-15. I²C Interface Switching Requirements(1) (2)

NO.	PARAMETER		MIN	MAX	UNIT
Slave High-Speed Mode					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	160		ns
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	60		ns
Slave Fast-Speed Mode					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	1.3		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	0.6		µs
Slave Standard Mode					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	4		µs

(1) The capacitive load is equivalent to:
100 pF in high-speed mode
400 pF in fast-speed mode
400 pF in standard mode
(2) SDA is equal to I2C.SR.SDA or I2C.CNTL.SDA
SCL is equal to I2C.SR.SCL or I2C.CNTL.SCL

7.5 Audio Interface: TDM/I2S Protocol

The TPS65951 acts as a master for the TDM and I2S interface or as a slave only for the I2S interface. If the TPS65951 is the master, it must provide the frame synchronization (TDM / I2S_SYNC) and bit clock (TDM / I2S_CLK) to the host processor. If it is the slave, the TPS65951 receives frame synchronization and bit clock.

The TPS65951 supports the I2S, TDM, left-justified, and right-justified data formats, but does not support the TDM slave mode.

7.5.1 I2S Right- and Left-Justified Data Format

Table 7-16 and Table 7-16 assume testing over the recommended operating conditions (see Figure 7-5 and Figure 7-6).

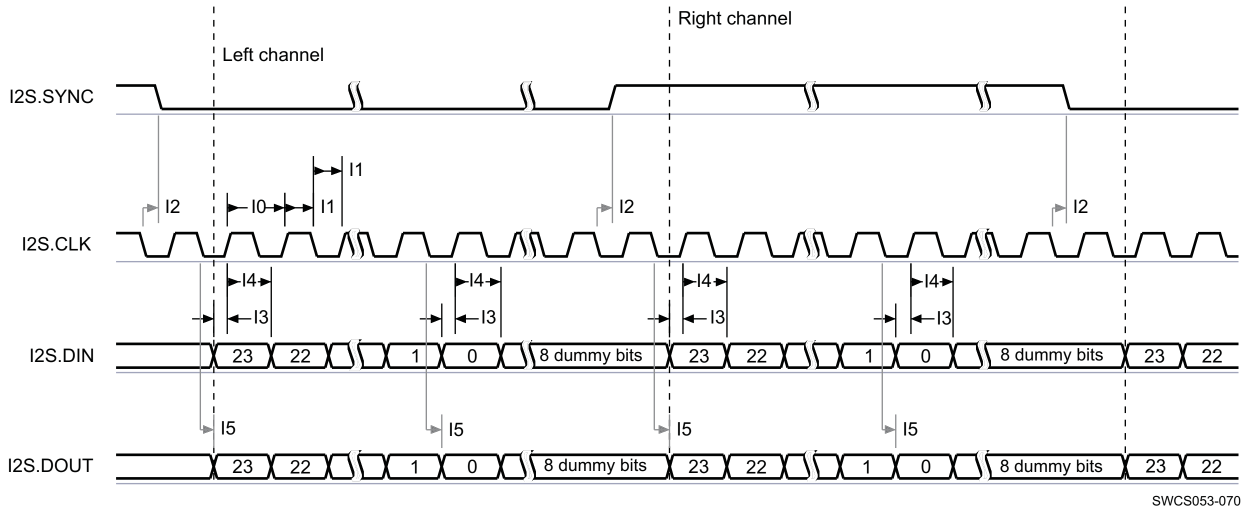


Figure 7-5. I2S Interface—I2S Master Model

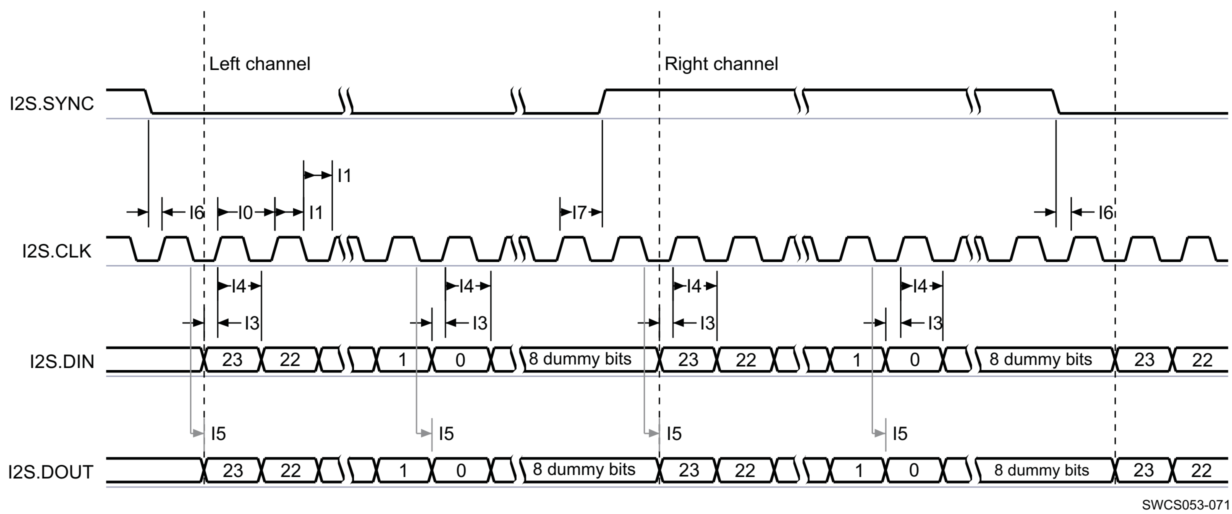


Figure 7-6. I2S Interface—I2S Slave Mode

The timing requirements below are valid on the following conditions of input slew and output load:

- Rise and fall time range of inputs (SYNC, DIN) is t_R/t_F = 1.0 ns/6.5 ns
- Capacitance load range of outputs (CLK, SYNC, DOUT) is C_{LOAD} = 1 pF/30 pF

The input timing requirements in Table 7-16 are given by considering a rising or falling time of 6.5 ns.

Table 7-16. I2S Interface—Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
Master Mode					
I3	$t_{su(DIN-CLKH)}$	Setup time, I2S.DIN valid to I2S.CLK high2	25		ns
I4	$t_{h(DIN-CLKH)}$	Hold time, I2S.DIN valid from I2S.CLK high.	0		ns
Slave Mode					
I0	$t_{c(CLK)}$	Cycle time, I2S.CLK(1)	1/64 × Fs		ns
I1	$t_{w(CLK)}$	Pulse duration, I2S.CLK high or low(2)	0.45 × P	0.55 × P	ns
I3	$t_{su(DIN-CLKH)}$	Setup time, I2S.DIN valid to I2S.CLK high	5		ns
I4	$t_{h(DIN-CLKH)}$	Hold time, I2S.DIN valid from I2S.CLK high.	5		ns
I6	$t_{su(SYNC-CLKH)}$	Setup time, I2S.SYNC valid to I2S.CLK high	5		ns
I7	$t_{h(SYNC-CLKH)}$	Hold time, I2S.SYNC valid from I2S.CLK high	5		ns

(1) Fs = 8 kHz to 48 kHz; 96 kHz for RX path only
(2) P = I2S.CLK period

The capacitive load for Table 7-17 is equivalent to 7 pF.

Table 7-17. I2S Interface—Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
Master Mode					
I0	$t_{c(CLK)}$	Cycle time, I2S.CLK(1)	1/64 × Fs		ns
I1	$t_{w(CLK)}$	Pulse duration, I2S.CLK high or low(2)	0.45 × P	0.55 × P	ns
I2	$t_{d(CLKL-SYNC)}$	Delay time, I2S.CLK falling edge to I2S.SYNC transition	–10	10	ns
I5	$t_{d(CLKL-DOUT)}$	Delay time, I2S.CLK falling edge to I2S.DOUT transition	–10	10	ns
Slave Mode					
I5	$t_{d(CLKL-DOUT)}$	Delay time, I2S.CLK falling edge to I2S.DOUT transition	0	20	ns

(1) Fs = 8 kHz to 48 kHz; 96 kHz for RX path only
(2) P = I2S.CLK period

7.5.2 TDM Data Format

Table 7-18 and Table 7-19 assume testing over the recommended operating conditions (see Figure 7-7).

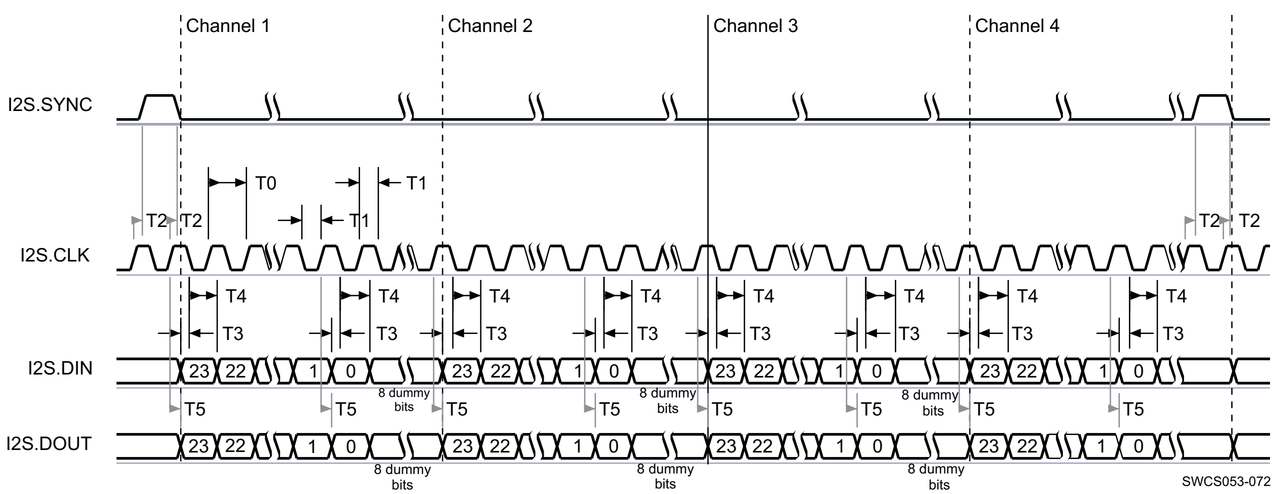


Figure 7-7. TDM Interface—TDM Master Mode

The timing requirements below are valid on the following conditions of input slew and output load:

- Rise and fall time range of inputs (SYNC, DIN) is t_R/t_F = 1.0 ns/6.5 ns
- Capacitance load range of outputs (CLK, SYNC, DOUT) is C_{LOAD} = 1 pF/30 pF

Table 7-18. TDM Interface Master Mode Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
T3	$t_{su(DIN-CLKH)}$	Setup time, TDM.DIN valid to TDM.CLK high	25		ns
T4	$t_{h(DIN-CLKH)}$	Hold time, TDM.DIN valid from TDM.CLK high	0		ns

Table 7-19. TDM Interface Master Mode Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
T0	$t_{c(CLK)}$	Cycle time, TDM.CLK (1)	1/64 × Fs		ns
T1	$t_{w(CLK)}$	Pulse duration, TDM.CLK high or low (2)	0.45 × P	0.55 × P	ns
T2	$t_{d(CLKL-SYNC)}$	Delay time, TDM.CLK rising edge to TDM.SYNC transition	–10	10	ns
T5	$t_{d(CLKL-DOUT)}$	Delay time, TDM.CLK rising edge to TDM.DOUT transition	–10	12	ns

(1) Fs = 8 kHz to 48 kHz; 96 kHz for RX path only
(2) P = TDM.CLK period

7.6 Voice PCM Interfaces

The PCM interface is intended to transfer voice data at 8-kHz (default narrowband mode) or 16-kHz (wideband mode) sample rates. The PCM interface can act as a slave or master. No PLL is used for the PCM interface, but dividers are used to derive the 8-kHz or 16-kHz clock from HFCLKIN (only when HFCLKIN = 26 MHz). If the system master clock is different from 26 MHz, voice PCM interface is not available.

Two modes are available for the PCM interfaces: Mode 1 (writing on the PCM_VCK rising edge) and Mode 2 (writing on the PCM_VCK falling edge).

Table 7-20 and Table 7-21 assume testing over the recommended operating conditions (see Figure 7-8 and Figure 7-9).

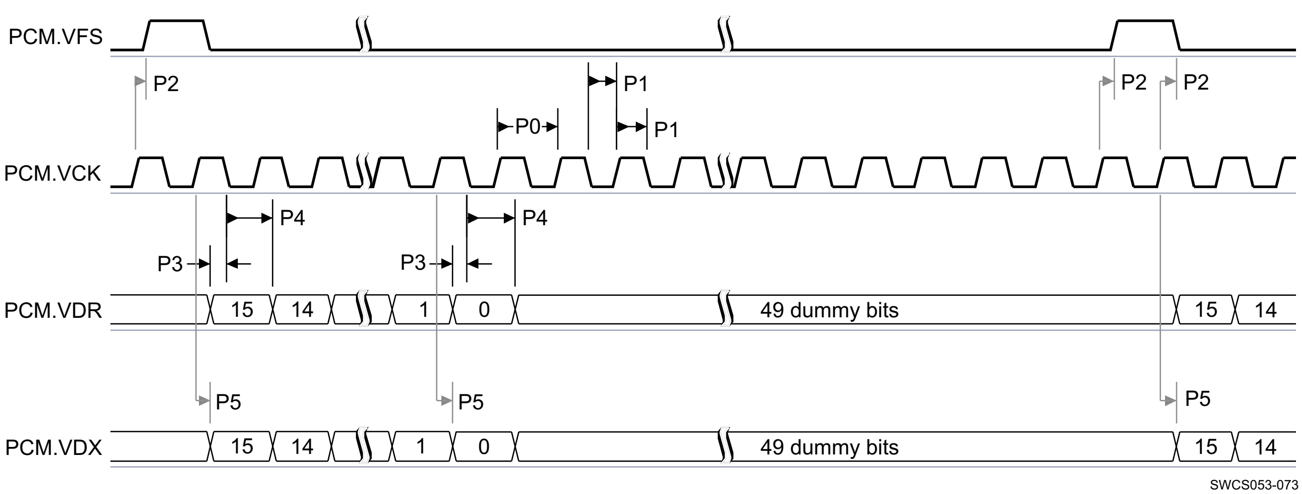


Figure 7-8. Voice PCM Interface—Master Mode (Mode 1)

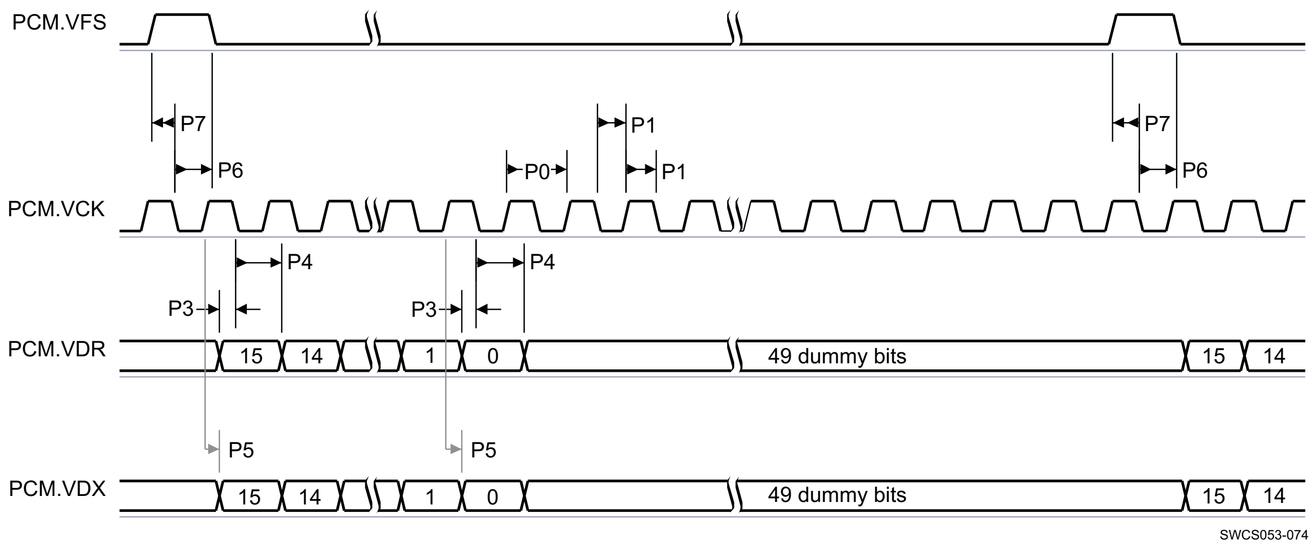


Figure 7-9. Voice PCM Interface—Slave Mode (Mode 1)

The timing requirements below are valid on the following conditions of input slew and output load:

- Rise and fall time range of inputs (SYNC, DIN) is t_R/t_F = 1.0 ns/6.5 ns
- Capacitance load range of outputs (CLK, SYNC, DOUT) is C_{LOAD} = 1 pF/30 pF

Table 7-20. Voice PCM Interface Timing Requirements (Mode 1)

NO.	PARAMETER		MIN	MAX	UNIT
Voice PCM Master Mode					
P3	$t_{su(VDR-VCK)}$	Setup time, PCM.VDR valid to PCM. VCK transition (1)	30		ns
P4	$t_{h(VDR-VCK)}$	Hold time, PCM.VDR valid from PCM.VCK transition (1)	0		ns
Voice PCM Slave Mode					
P0	$t_{c(VCK)}$	Cycle time, PCM.VCK (2)	1/(33 to 65 × Fs)		ns
P1	$t_{w(VCK)}$	Pulse duration, PCM.VCK high or low (3)	0.45 × P	0.55 × P	ns
P3	$t_{su(VDR-VCK)}$	Setup time, PCM.VDR valid to PCM. VCK transition (1)	10		ns
P4	$t_{h(VDR-VCK)}$	Hold time, PCM.VDR valid from PCM. VCK transition (1)	5		ns
P6	$t_{h(VFS-VCK)}$	Hold time, PCM.VFS valid from PCM.VCK transition (1)	5		ns
P7	$t_{SU(VFS-VCK)}$	Setup time, PCM.VFS valid to PCM. VCK transition (1)	10		ns

(1) Writing on PCM.VCK rising edge (Mode1) and writing on PCM.VCK falling edge (Mode 2).
(2) Fs = 8 kHz or 16 kHz
(3) P = PCM.CLK period

Table 7-21. Voice PCM Interface Switching Characteristics (Mode 1)

NO.	PARAMETER		MIN	MAX	UNIT
Voice PCM Master Mode					
P0	$t_{c(VCK)}$	Cycle time, PCM.VCK (1)	1/65 × Fs		ns
P1	$t_{w(VCK)}$	Pulse duration, PCM.VCK high or low (2)	0.45 × P	0.55 × P	ns
P2	$t_{d(VCK-VFS)}$	Delay time, PCM.VCK transition to PCM.VFS transition (3)	–10	10 + Pvoice	ns
P5	$t_{d(VCL-VDX)}$	Delay time, PCM.VCK transition to PCM.VDX transition	–10	10	ns
Voice PCM Slave Mode					
P5	$t_{d(VCL-VDX)}$	Delay time, PCM.VCK transition to PCM.VDX transition	0	20	ns

(1) Fs = 8 kHz or 16 kHz
(2) P = PCM.CLK period
(3) When TPS65951 is master, the PCM.VFS is delivered 1 cycle time of 26-MHz voice clock (Pvoice=38.4 ns) after the PCM.VCK rising edge.

7.7 JTAG Interfaces

The TPS65951 JTAG TAP controller handles standard IEEE JTAG interfaces. This section describes the timing requirements for the tools used to test the TPS65951 power management.

The JTAG/TAP module provides a JTAG interface according to IEEE Std1149.1a. This interface uses the four I/O pins TMS, TCK, TDI, and TDO. The TMS, TCK, and TDI inputs contain a pullup device, which makes their state high when they are not driven. The output TDO is a 3-state output, which is high impedance except when data is shifted between TDI and TDO.

- TCK is the test clock signal.
- TMS is the test mode select signal.
- TDI is the scan path input.
- TDO is the scan path output.

TMS and TDO are multiplexed at the top level with the CPIO0 and CPIO1 pins. The dedicated external TEST pin switches from functional mode (GPIO0/GPIO1) to JTAG mode (TMS/TDO). The JTAG operations are controlled by a state-machine that follows the IEEE Std1149.1a state diagram. This state-machine is reset by the TPS65951 internal power-on reset. A test mode is selected by writing a 6-bit word (instruction) into the instruction register and then accessing the related data register.

Table 7-22 and Table 7-23 assume testing over the recommended operating conditions (see Figure 7-10).

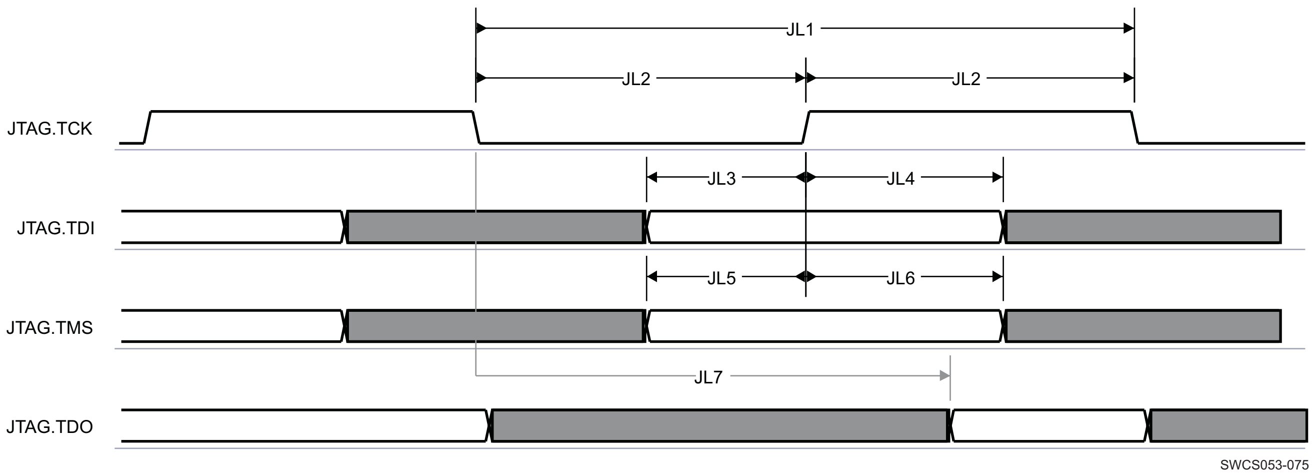


Figure 7-10. JTAG Interface Timing

The input timing requirements are given by considering a rising or falling edge of 7 ns.

Table 7-22. JTAG Interface Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
		Clock			
JL1	$t_{c(TCK)}$	Cycle time, JTAG.TCK period	30		ns
JL2	$t_{w(TCK)}$	Pulse duration, JTAG.TCK high or low(1)	0.48 × P	0.52 × P	ns
		Read Timing			
JL3	$t_{su(TDIV-TCKH)}$	Setup time, JTAG.TDI valid before JTAG.TCK high	8		ns
JL4	$t_{h(TDIV-TCKH)}$	Hold time, JTAG.TDI valid after JTAG.TCK high	5		ns
JL5	$t_{su(TMSV-TCKH)}$	Setup time, JTAG.TMS valid before JTAG.TCK high	8		ns
JL6	$t_{h(TMSV-TCKH)}$	Hold time, JTAG.TMS valid after JTAG.TCK high	5		ns

(1) P = JTAG.TCK clock period

The capacitive load is equivalent to 35 pF.

Table 7-23. JTAG Interface Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
Write Timing					
JL7	$t_{d(TCK-TDOV))}$	Delay time, JTAG, TCK active edge to JTAG.TDO valid	0	14	ns

8 Battery Interface

8.1 General Description

8.1.1 BCI Overview

The TPS65951 has a battery charger interface (BCI) for complete battery management. The main function of the BCI is to control external chargers. It supports external chargers of 20 V absolute maximum. The BCI manages charger detection, battery pack presence checks, and control enable of external USB chargers.

The detection of battery presence is done by a comparator that monitors the ADCIN0 signal in the MADC. The battery pack has a pull down resistor, and the TPS65951 has a current source in the line. MANU_BRIX pin is used for battery removal detection and generates an interrupt upon battery removal.

The battery can be monitored using the 10-bit ADC converter from the MADC module to measure the battery voltage, battery temperature, battery type, and USB device input voltage.

8.1.2 Battery Backup Overview

The TPS65951 implements a backup mode, in which the backup battery keeps the RTC clock running. If the backup battery is rechargeable, it can be recharged from the main battery.

When the main battery is below 2.7 V or is removed, the backup battery powers the backup if the backup battery voltage is greater than 1.8 V. The backup domain powers up the following:

- The internal 32.768-kHz oscillator
- The RTC
- The hash table (20 registers of 8 bits each)
- Eight general-purpose storage registers
- Backup domain low power
- Power-on-reset (PORZ) circuit and VBRTC power state machine (PSM)

8.2 Block Diagram

BCI related blocks are shown in Figure 8-1.

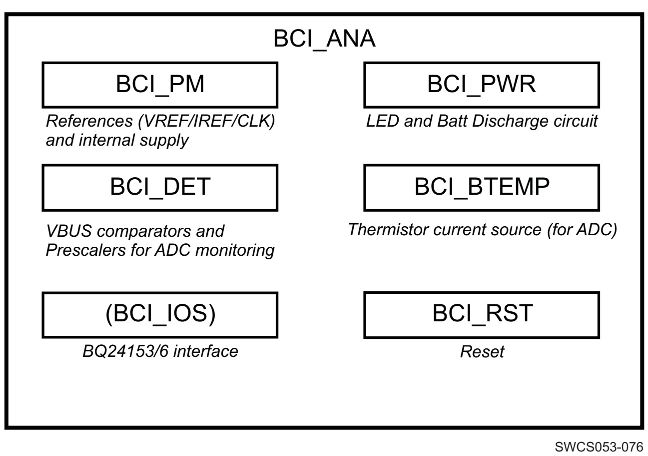


Figure 8-1. Battery Charger Block Diagram

8.2.1 BCI References (BCI_PM)

BCI_PM includes the references (VREF, IREF, CLK) and internal supplies.

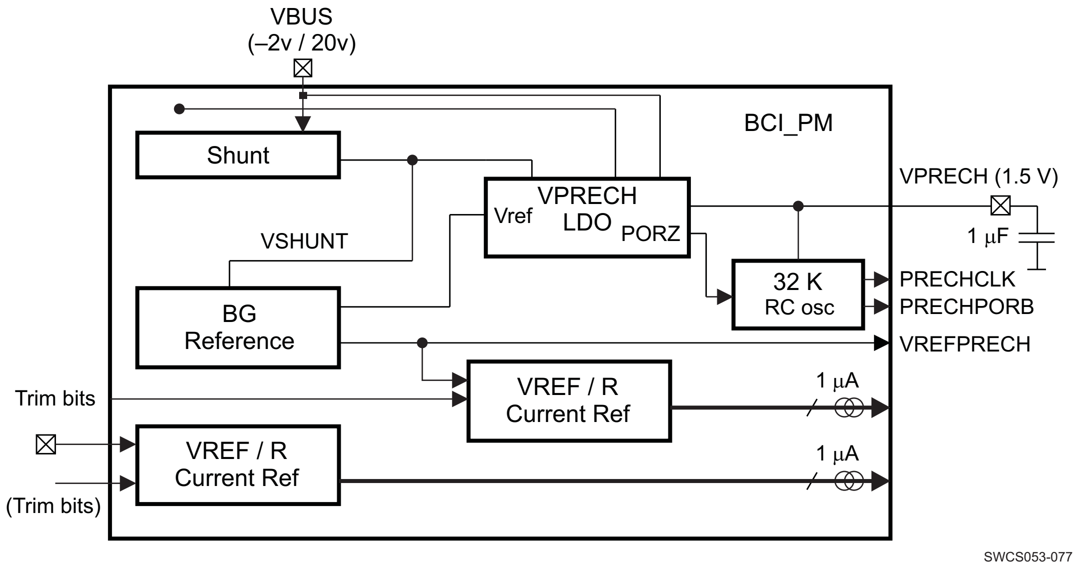


Figure 8-2. BCI References Block Diagram

Table 8-1. References Electrical Conditions

PARAMETER	CONDITIONS	SPECIFICATION			UNITS
		MIN	TYP	MAX	
VPRECH Capacitor		0.8	1	2.7	µF
VPRECH Capacitor ESR		10		600	mΩ
Charger (VBUS) required level for	When the charger voltage is in-between these limits: VPRECH_PORZ = 1 VPRECH > 1.35 V	3		20	V
Shunt Regulator Output	VBUS between 3 V and 20 V			3.6	V
VREFPRECH(1)	for ±4 sigma		0.75		V
VPRECH_PORZ threshold	VPRECH_PORZ toggles from 0 to 1 and 1 to 0 according to this VPRECH-LDO output value.	1.2	1.3		V
VPRECH	LDO output with 10 mA total load (TPS65951 < 1 mA)	1.35	1.5	1.65	V
Oscillator Frequency	Internal RC oscillator frequency	26	33	40	kHz

(1) VREFPRECH reaches 99% of its final value when VPRECH_PORZ rises to 1.

8.2.2 Thermistor Current Source for GPADC (BCI_BTEMP)

Table 8-2. ADCIN1 Current Source Electrical Parameters

PARAMETER	CONDITIONS	SPECIFICATION			UNITS
		MIN	TYP	MAX	
ADCIN1 current source (SYSACTIV = 1)(1)	Absolute level after trim	9.50	10.0	10.5	μA
	Relative variation over temperature and supplies	–1.5%		1.5%	

(1) SYSACTIV is an internal signal, corresponds to NRESPWRON.

8.2.3 BCI Power (BCI_PWR)

BCI_PWR includes the LED and battery discharge circuits.

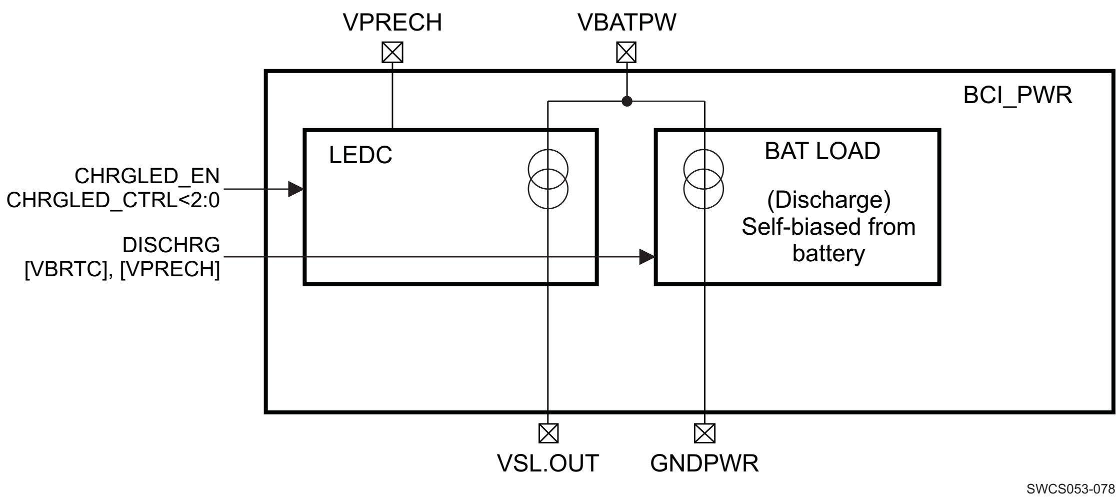


Figure 8-3. Charging LED/Battery Discharge Driver Block Diagram

Table 8-3. Charging LED/Battery Discharge Electrical Characteristics

PARAMETER	CONDITIONS	SPECIFICATION			UNITS
		MIN	TYP	MAX	
BCI_PWR					
Charge LED battery range	VBAT level during LED enable	1.8		4.8	V
Charge LED voltage over current source		0.2		VBAT – 0.4	V
LED current	LEDCTRL<2:0> = 000	1.8	3.5	5	mA
	LEDCTRL<2:0> = 001	0.4	0.875	1.25	mA
	LEDCTRL<2:0> = 010 (default)	0.9	1.75	2.5	mA
	LEDCTRL<2:0> = 011	3.5	7	10	mA
	LEDCTRL<2:0> = 100	7	14	20	mA
Battery load	enabled when battery is detached VBAT from 1.8 V to 4.5 V	15	30	60	mA

Table 8-4. Battery Discharge and Charging LED Timing

Requirement	PARAMETER	Nb Clock	Test Conditions	MIN	TYP	MAX	UNIT
Minimum 30 ms	BATT_PRES_DEB_VPRECH	1344		33.6	40.7	51.7	ms
Minimum 30 ms	BATT_PRES_DEB_VBRTC	983		30		30	ms
Minimum 2 s	BATTERY_DISCHARGE_TIME	89600	Precharge (1)	2.24	2.72	3.45	s
			ACTIVE/SLEEP mode, WAIT-ON/BACKUP mode without charger (2)	2.73		2.73	s
Minimum 150 ms	LEDC_PULSE	6720	BACKUP/WAIT-ON mode (1)	168	204	259	ms
			ACTIVE/SLEEP mode (2)	205		205	ms
Minimum 1 s	LEDC_1S	33376	BACKUP/WAIT-ON mode (1)	0.83	1.01	1.28	s
			ACTIVE/SLEEP mode (2)	1.02		1.02	s
Minimum 1, 5 s	LEDC_1S5	47680	BACKUP/WAIT-ON mode (1)	1.19	1.44	1.83	s
			ACTIVE/SLEEP mode (2)	1.46		1.46	s
Minimum 2 s	LEDC_2S	61984	BACKUP/WAIT-ON mode (1)	1.55	1.88	2.38	s
			ACTIVE/SLEEP mode (2)	1.89		1.89	s

(1) Clocked on 32K RC based oscillator, cover also transition between wait-on and active mode.
(2) Clocked on 32K Xtal oscillator

8.2.4 Battery Removal

If battery removal is detected, the battery node is discharged. The BATT_PRES signal is level-shifted, and the signal is debounced. The debounce time equals BATT_PRES_DEB_VPRECH (= 40.7 ms typical) in the VPRECH domain (during PRECHARGE state), and BATT_PRES_DEB_VBRTC (= 30 ms) in the VBRTC domain (during the ACTIVE charging state). After debouncing, discharging of the battery node starts, and discharging (SINK) is kept enabled for the time specified in BATTERY_DISCHARGE_TIME register. Discharging of the battery node is implemented with a current sink, mirrored from a current reference block that is self-supplied by the battery domain. The BATT_PRES signal also propagates to the MANU_BRIX pin indicating that the battery pack has been removed, and to the interrupt system. There is a resynchronization of three periods of the 3.2-MHz clock before interrupts are generated.

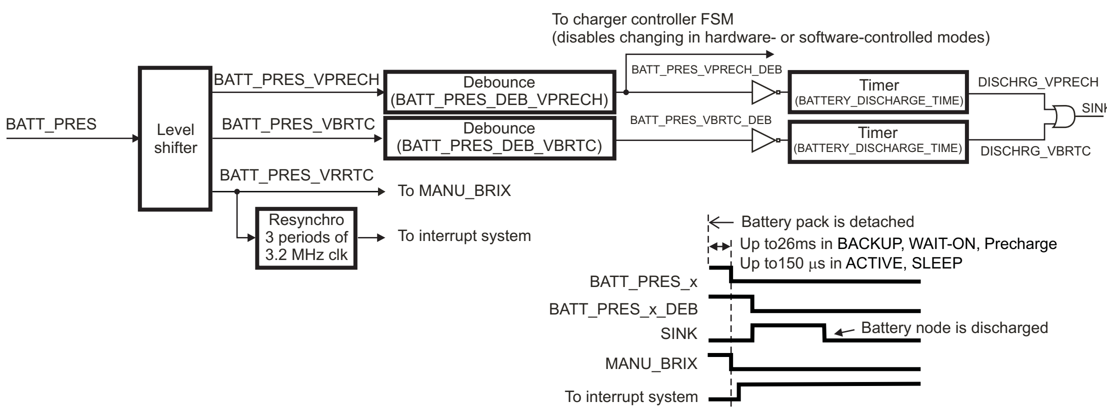


Figure 8-4. Battery Removal and Discharge Control

8.2.5 BCI VBAT-VBUS Detection (BCI_DET)

BCI_DET includes the VBUS comparators and prescalers for ADC monitoring.

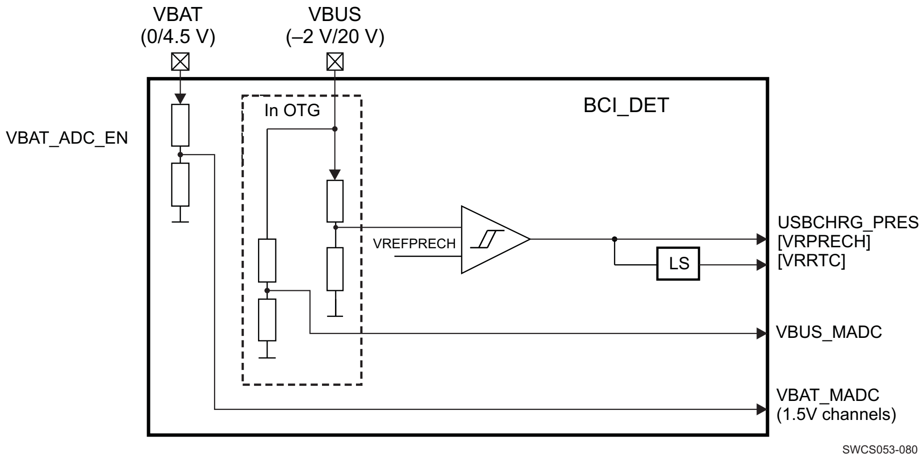


Figure 8-5. Charger Detection Block Diagram

Table 8-5. Charger Detection Electrical Characteristics

PARAMETER	CONDITIONS	SPECIFICATION			UNITS
		MIN	TYP	MAX	
BCI_DET					
VBUS Presence USBCHRG_PRES	low to high	3.1	3.35	3.7	V
	high to low	3.05	3.25	3.7	V
	hysteresis	25			mV

Table 8-6. MADC Input Attenuation

PARAMETER	CONDITIONS	SPECIFICATION			UNITS
		MIN	TYP	MAX	
VBAT to MADC input attenuation	VBAT up to 4.5 V (1)		0.25		V/V
VBUS to MADC input attenuation	VBUS up to 6.5 V (2)		3/14		V/V

(1) VBAT measurement through ADC accuracy is ±8% for VBAT between 3 V and 4.7 V.
(2) VBUS measurement through ADC accuracy is ±10% for VBUS between 3 V and 6.5 V. If the measured code is 1023 (ADC upper saturation), VBUS is > 6.5 V.

8.2.6 *BCI Interface (BCI_IOS)*

The BCI_IOS is the digital BQ24153/6 interface.

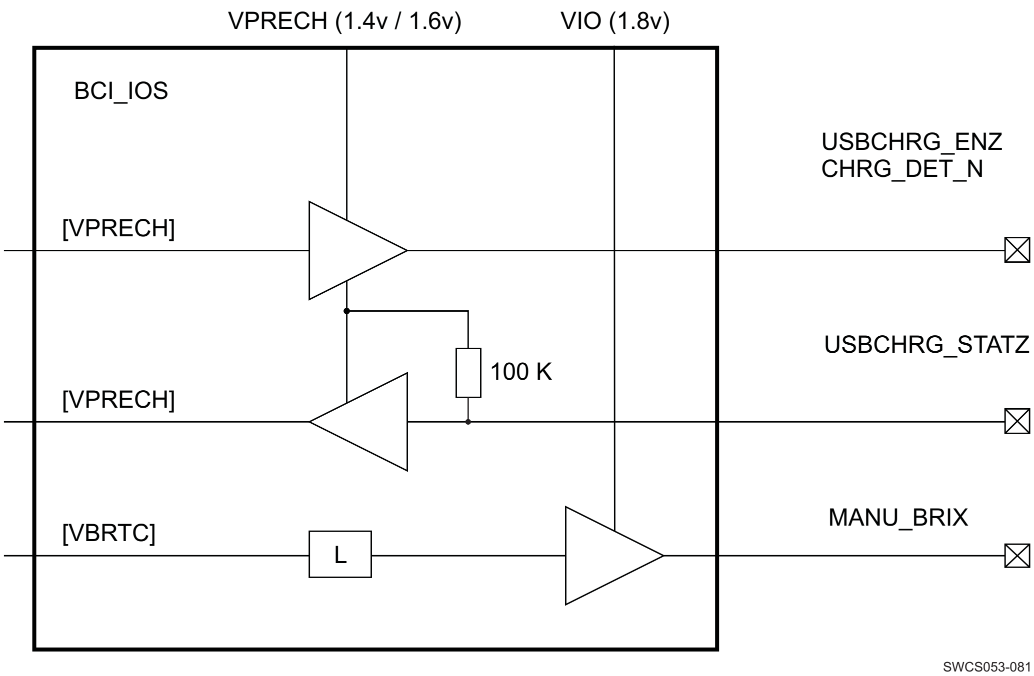


Figure 8-6. Battery Charger Digital Interface

8.2.7 *External USB Charger Control*

8.2.7.1 USB Charger Detection

Table 8-7. USB Charger Detection Debounce Timing

USB CHARGER DETECTION							
REQUIREMENT	**PARAMETER**	**Nb CLOCK**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Minimum 10 ms	DEBVBUS_TIME	448	Backup/Wait-on mode (1)	11.2	13.6	17.2	ms
			Active/Sleep mode (2)	13.7		13.7	ms

(1) Clocked on 32K RC based oscillator, also covers transition between wait-on and active mode.
(2) Clocked on 32K Xtal oscillator

8.2.7.1.1 USB Charger Detection Electrical Characteristics

Table 8-8. Electrical Specifications – Voltages

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Logic Threshold	$V_{CHGD_SERX_DP_DM}$		0.8	2	V
D+ Source Voltage	V_{DP_SRC}	Output current > 250 µA	0.5	0.675	V
Data Detect Voltage	V_{DAT_REF}		0.25	0.4	V

Table 8-9. Electrical Specifications – Currents

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Data Contact Detect Current Source	I_{DP_SRC}		7	13	µA
D- Sink Current	I_{DM_SINK}		50	150	µA

Table 8-10. Electrical Specifications – Resistances

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
D+ Pull-down resistance	R_{DP_DWN}		14.25	24.8	kΩ
D- Pull-down resistance	R_{DM_DWN}		14.25	24.8	kΩ

Table 8-11. Wait and Debounce Timing

USB CHARGER DETECTION							
REQUIREMENT	PARAMETER	Nb CLOCK	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum 200 us	D+ Current source on-time TIDP_SRC_ON	8	Backup/Wait-on mode (1)	200	242.2	307.7	µs
			Active/Sleep mode (2)	244.1		244.1	µs
	VDx_SRC comparator debounce time TVDPSRC_DEB	1344	Backup/Wait-on mode (1)	33.6	40.7	51.7	ms
			Active/Sleep mode (2)	41		41	ms
	Charger detect SERX debounce time TCHGD_SERX_DEB	1792	Backup/Wait-on mode (1)	44.8	54.3	68.9	ms
			Active/Sleep mode (2)	54.7		54.7	ms
Minimum 40 ms	D+ Voltage source on-time TVDP_SRC_ON	1792	Backup/Wait-on mode (1)	44.8	54.3	68.9	ms
			Active/Sleep mode (2)	54.7		54.7	ms
Minimum 40 ms	D+ Voltage source off to high current TVDP_SRC_HICRNT	1792	Backup/Wait-on mode (1)	44.8	54.3	68.9	ms
			Active/Sleep mode (2)	54.7		54.7	ms
Minimum 2 s	DATA_CONTACT_DETECT Timeout TDCD_TIMEOUT	89600	Backup/Wait-on mode (1)	2.24	2.72	3.45	s
			Active/Sleep mode (2)	2.73		2.73	s

(1) Clocked on 32K RC based oscillator, also covers transition between wait-on and active mode.
(2) Clocked on 32K Xtal oscillator

8.2.7.2 Internal Charger Error Signal (USBCHRG_STATZ)

Table 8-12. Error Delay Timing

BATTERY CHARGER FSM							
REQUIREMENT	PARAMETER	Nb CLOCK	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum 100 ms	CHG_ERROR100MS	4480	BACKUP/WAIT-ON mode(1)	112.0	135.8	172.3	ms
			ACTIVE/SLEEP mode(2)	136.7		136.7	ms
Minimum 2.5s	CHG_ERROR2S5	112000	BACKUP/WAIT-ON mode(1)	2.8	3.4	4.3	s
			ACTIVE/SLEEP mode(2)	3.4		3.4	s

(1) Clocked on 32K RC based oscillator, also covers transition between wait-on and active mode.
(2) Clocked on 32K Xtal oscillator

8.2.7.3 Battery Discharge Timimg

Table 8-13. Battery Discharge Timing

BATTERY DISCHARGE							
REQUIREMENT	PARAMETER	Nb CLOCK	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum 2 s	BATTERY_DISCHARGE_TIME	89300	Precharge(1)	2.24	2.72	3.45	s
			ACTIVE/SLEEP mode, WAIT-ON/BACKUP mode without charger(2)	2.73		2.73	s

(1) Clocked on 32K RC based oscillator, also covers transition between wait-on and active mode.
(2) Clocked on 32K Xtal oscillator

8.2.7.4 Watchdog

Table 8-14. Watchdog Timing

BATTERY CHARGER WATCHDOG							
REQUIREMENT	PARAMETER	Nb CLOCK	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum 32 mn	WATCHDOGHW_32MN	36864000	BACKUP/WAIT-ON mode(1)	15.4	18.6	23.6	mn
Maximum 16 mn	WATCHDOGHW_16MN	18432000	BACKUP/WAIT-ON mode(1)	7.7	9.3	11.8	mn
Maximum 16 s	CHG_WATCHDOG 16S	524283	ACTIVE/SLEEP mode(2)	16.0		16.0	s
Maximum 32 s	CHG_WATCHDOG 32S	1048566	ACTIVE/SLEEP mode(2)	32.0		32.0	s
Maximum 64 s	CHG_WATCHDOG 64S	2097131	ACTIVE/SLEEP mode(2)	64.0		64.0	s
Maximum 127 s	CHG_WATCHDOG 127S	4161494	ACTIVE/SLEEP mode(2)	127.0		127.0	s

(1) Clocked on 32K RC based oscillator, also covers transition between wait-on and active mode.
(2) Clocked on 32K Xtal oscillator

8.3 External Charger Control

The BCI module has two modes, hardware (also called precharge) and software mode:

- Hardware mode (precharge mode): Charging is controlled by three finite state-machines (FSMs):
  - Battery charger watchdog FSM
  - USB-charger detection FSM
  - Battery charger control FSM

  Charger control is in hardware mode when a charger is plugged and the device is in NO SUPPLY, WAIT-ON, or BACKUP state. Charger control also remains under hardware control when the device is in ACTIVE or SLEEP state and the BCC_CTRL2[0] CHGMODE_SW bit is 0.
- Software mode: The BCI is under software control when the device is in ACTIVE or SLEEP state and the BCC_CTRL2[0] CHGMODE_SW bit is set to 1.

The focus of this document is on the hardware mode which needs no user action to control the internal device registers.

8.3.1 USB Charger Detection

To function, the USB charger detection requires a valid VBUS signal and BATTERY_PRESENCE signal. The charger detection FSM detects two types of USB chargers, USB 100-mA charger and USB 500-mA charger. Two signals (USB100_P and USB500_P) are the result of the USB charger detection FSM. The status of the USB100_P and USB500_P signals can be read from the USB_CHRG_CTRL2[1:0] bit field.

- USB100_P: Valid 100-mA charger (VBUS supplier) is detected.
- USB500_P: Valid 500-mA charger (USB charging port) is detected.

USB100 refers to standard downstream port (SDP) and USB500 refers to charging downstream port (CDP) or dedicated charging port (DCP).

The charger detection result is input to the battery charger control FSM. Two signals control the external charger:

- USBCHRG_ENZ: (Active low) enables the external USB charger.
- CHRG_DET_N: When CHRG_DET_CFG is 1 (default), then CHRG_DET_N = 1 when a USB 500-mA charger is detected, and CHRG_DET_N = 0 when a USB 100-mA charger is detected.

In hardware mode, charging stops when a watchdog time-out event occurs (WATCHDOG_EVENT = 1), a battery presence check fails (BATTERY_PRESENCE = 0), or when no charger is present (VPRECH_PORZ signal is 0). Hardware mode (precharge) charging also stops when it is under software control and charging stops if USB100 charging is ongoing in hardware mode when a switch-on (WAIT-ON-to-ACTIVE) state transition occurs.

In hardware mode, a read of these register bits (BCC_CTRL2[3:1]) gives the status of the corresponding signals.

- External input signal:
  - USBCHRG_STATZ: Status of USB charger (from BQ24153)
- Definition (from BQ24153/6 device):
  - In case of noncharging: Pull up to supply (VPRECH)
  - In case of charging: 0
  - In case of fault: (see plot below): STATZ Error Frame

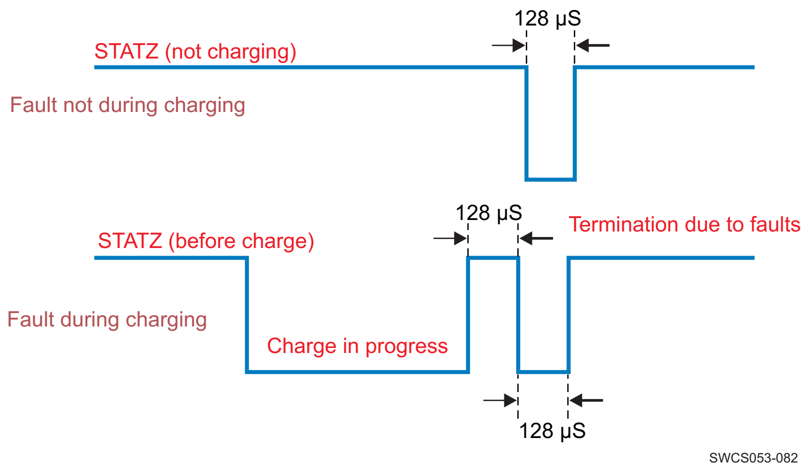


Figure 8-7. Charging Error Frame

8.3.2 Battery Charger Control State Machine

If the VPRECH_PORZ or BATTERY_PRESENCE signal is not asserted, all digital charger logic is reset, and the charger is disabled.

If the WATCHDOG_EVENT signal or BCC_CTRL[0] SW_CHRGOFF bit is asserted, all logic is cleared and all chargers are disabled through the PRECHARGE_OFF signal. The PRECHARGE_OFF signal is also set if the BCC_CTRL2[0] CHGMODE_SW bit is set to 1.

There are four output signals from the battery charger control FSM:

- USBCHRGSTM_EN: Sets the USBCHRG_EN signal when in hardware mode:
  - 0: USB charger is disabled
  - 1: USB charger is enabled.
- CHRGSTM_DET: Sets the CHRG_DET signal when in hardware mode (selects the USB charger current):
  - 0: 100-mA charger type
  - 1: 500-mA charger type
- RESET_WATCHDOG_HW: Resets the battery charger watchdog when in hardware mode:
  - 0: Watchdog is not reset.
  - 1: Watchdog is reset

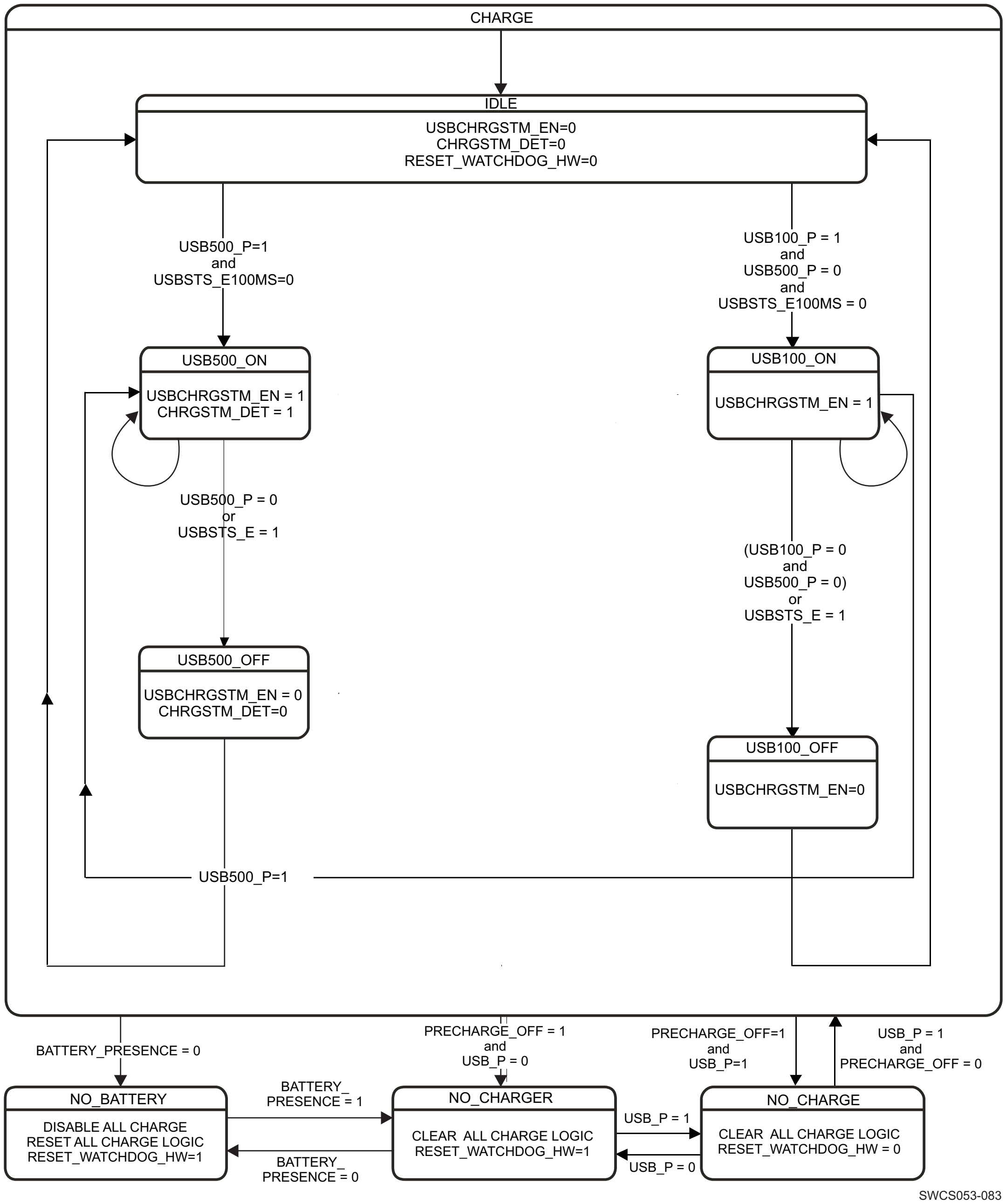


Figure 8-8. Battery Charger Control State Machine

Priority

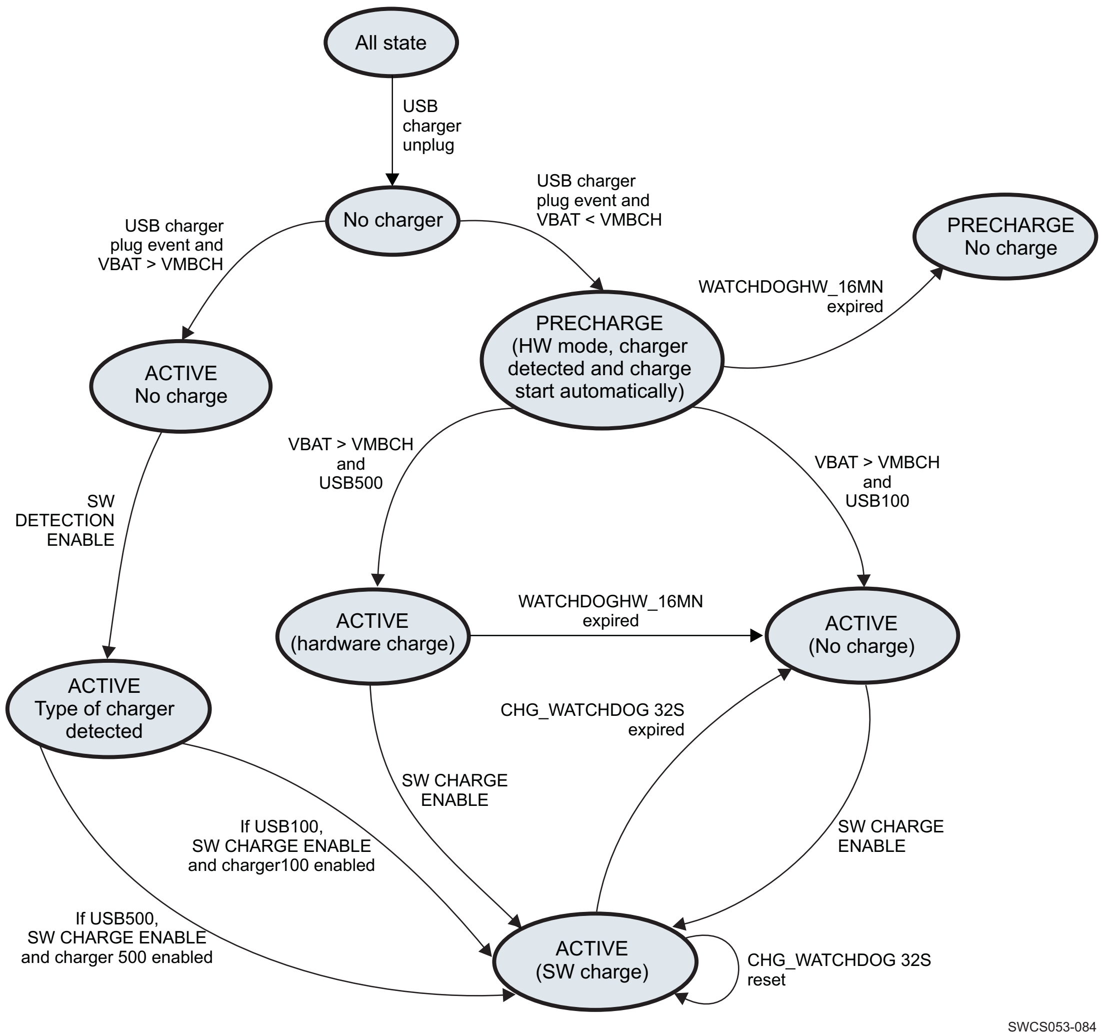
The USB500 charger has priority over the USB100 charger. If a charger error happens during charging (using the USBSTS_E signal), charging from a defective charger is disabled and priority is given to the next priority charger for CHG_ERROR2S5 (3.4 s typical). This is the time left for the charger to recover from the error using the USBSTS_ERROR signal.

USB Charger Detection

The status of the USB charger detection can be updated during charging. USB 100-mA charging must be stopped if the USB charger is detected (USB100_P falling, and USB500_P rising). To avoid the disabling and enabling of the USB charger, the USBCHRGSTM_EN signal is not cleared and the state-machine goes into USB500_ON state.

8.3.3 Charger Watchdog

In hardware mode, the battery will not be charged for more than WATCHDOGHW_16MN (set to '1' by default, 16 minutes). The charger watchdog is activated and the counter starts when a charger is enabled (USBCHRG_ENZ=0). The charger watchdog counter stars when charging starts and runs as long as a charger is connected. The charger watchdog is reset when no charger is connected or no battery is present. When charger watchdog reaches it time out value all chargers are disabled.



NOTE:

1. SW DETECTION ENABLE is done by setting BCC_CTRL2[4] SW_USB_DET_EN bit to 1. FSM updates the register bits in BCC_STS[1:0]USB_DET_STS that indicate the type of charger.
2. SW CHARGE ENABLE is done by setting BCC_CTRL2[1] SW_USBCHRG_EN bit to 1. BCC_CTRL2[0]CHGMODE_SW should be 1 prior to setting SW_USBCHRG_EN to 1.

Figure 8-9. Charging Flow chart

9 MADC

9.1 General Description

The TPS65951 shares the MADC resource between the host processors present in the system (hardware and software conversion mode) and the battery charger interface included on the TPS65951. Therefore, it has to:

- Manage potential concurrent requests of conversions and priority between the different resource users
- Flag, using interrupt signals, the end-of-sequence of conversions
- Grant quarter-bit accuracy for modem conversion of battery voltage

The quarter-bit accurate start signal is provided through a STARTADC from the host processor (real-time conversion).

The MADC generates interrupt signals sent to the host processors. Interrupts are handled primarily by its internal secondary interrupt handler and secondly at the upper level (outside MADC module) by the TPS65951 interrupt primary handler. The MADC indicates to the BCI module, via a data ready signal, that the conversion results are available.

9.2 Main Electrical Characteristics

Table 9-1. Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10		Bit
Input dynamic range for external input	Except ADCIN0 and ADCIN1 and internal MADC input (range from 0 V to 1.5 V)	0		2.5	V
MADC voltage reference			1.5		V
Differential nonlinearity		–1		1	LSB
Integral nonlinearity	Best fitting. For all channels (except ADCIN2 through ADCIN7 channels)	–2		2	LSB
Integral nonlinearity for ADCIN2, ADCIN3, and ADCIN7	Best fitting for Codes 230 to Max	–2.5		2.5	LSB
	Best fitting taking into account offset of 25 LSB	–4.5		4.5	LSB
Offset (best fitting)	For channels 0 , 1 and 10	–5		5	mV
	For other channels	–28.5		28.5	mV
Input capacitor C_{BANK}		6		10	pF
Input current leakage (for all 16 internal or external inputs)				1	μA

9.3 Channel Voltage Input Range

Table 9-2. MADC Analog Input Range and Prescaler Divide Ratio

MADC CHANNEL	INT/EXT	ANALOG INPUT RANGE (V)		PRESCALER			
				OUTPUT RANGE (V)		DIVIDER RATIO	NOTE
		MIN	TYP	MIN	MAX		
ADCIN0: Battery Detection	External	0	1.5	N/A	N/A	1	No prescaler
ADCIN1: BCI only, Battery temperature	External	0	1.5	N/A	N/A	1	No prescaler
ADCIN2: General-purpose input(1)	External	0	2.5	0	1.5	0.6	Fed through a common prescaler Rdivider = 11.4 kΩ/19 kΩ (typ)(2)
ADCIN3: General-purpose input(1)	External	0	2.5	0	1.5	0.6	
ADCIN7: General-purpose input(1)	External	0	2.5	0	1.5	0.6	
ADCIN8: VBUS voltage (VBUS)	Internal	0	6.5	0	1.5	3/14	Prescaler in USB subchip. Rdivider = 6 × 2.76 kΩ/28 × 2.76 kΩ (typ)(2)
ADCIN9: Backup battery voltage (BKBAT)	Internal	1.8	3.3	0.6	1.1	1/3	Prescaler in power subchip.(3) Rdivider = 212 kΩ/636 kΩ (typ)(4)
ADCIN10: Reserved	Internal	N/A	N/A	N/A	N/A	N/A	
ADCIN12: Main battery voltage (VBAT)	Internal	2.7	4.7	0.675	1.175	0.25	Prescaler in BCI module. Rdivider = 9.85 kΩ/4 × 9.85 kΩ (typ)(2)
ADCIN13: Reserved	Internal	N/A	N/A	N/A	N/A	N/A	
ADCIN14: Reserved	Internal	N/A	N/A	N/A	N/A	N/A	
ADCIN15:Reserved	Internal	N/A	N/A	N/A	N/A	N/A	

(1) General-purpose inputs have to be tied to ground when TPS65951 internal power supplies (VINTANA1 and VINTANA2) are off.
(2) Tolerance for resistors-type (PL_HR): ±12%
(3) To enable prescaler for ch9, BKBAT charging needs to be enabled (BB_CFG[BBCHEN] = 1). If BKBAT charging is not enabled, prescaler output for ch9 will be 0.
(4) Tolerance for resistors-type (PL_VHSR): ±19%

9.3.1 Sequence Conversion Time

Table 9-3 summarizes the sequence conversion timing characteristics. Figure 9-1 shows one conversion sequence general timing diagram.

Table 9-3. Sequence Conversion Timing Characteristics

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
F	Running frequency		1		MHz
T = 1/F	Clock period		1		µs
N	number of analog inputs to convert in a single sequence	0		16	
Tstart	SW1, SW2 or USB asynchronous request or real-time STARTADC request	3		4	µs
Tsettling time	Settling time to wait before sampling a stable analog input (capacitor bank charge time). Tsettling is calculated from the max((Rs + Ron) × Cbank) of the 16 possible input sources (internal or external). Rs and Cbank are defined in Table 9-1 and Ron is the resistance of the selection analog input switches (5 kΩ). This time is software programmable by AQUISITION register, default value is 12 µs.	5	12	1716	µs
Tstartsar	The successive approximation registers ADC start time		1		µs
Tadc time	The successive approximation registers ADC conversion time		10		µs
Tcapture time	Tcapture time is the conversion result capture time.		2		µs
Tstop		1		2	µs
Full Conversion Sequence Time	Only One Channel (N = 1)(1)	22		39	µs
	All Channels (N = 16)(1)	352		624	
Conversion Sequence Time	Without Tstart and Tstop: Only One Channel (N = 1)(1)	18		33	µs
	Without Tstart and Tstop: All channels (N = 16)(1)	288		528	
STARTADC pulse duration	STARTADC Period is T	0.33			µs

(1) Total Sequence Conversion Time General Formula: Tstart + N × (1 + Tsettling + Tadc + Tcapture) + Tstop.

This table is illustrated in Figure 9-1. The parameter "*Busy*" indicates that a conversion sequence is running, and the parameter "*channel N result register*" corresponds to the result register of RT/GP selected channel.

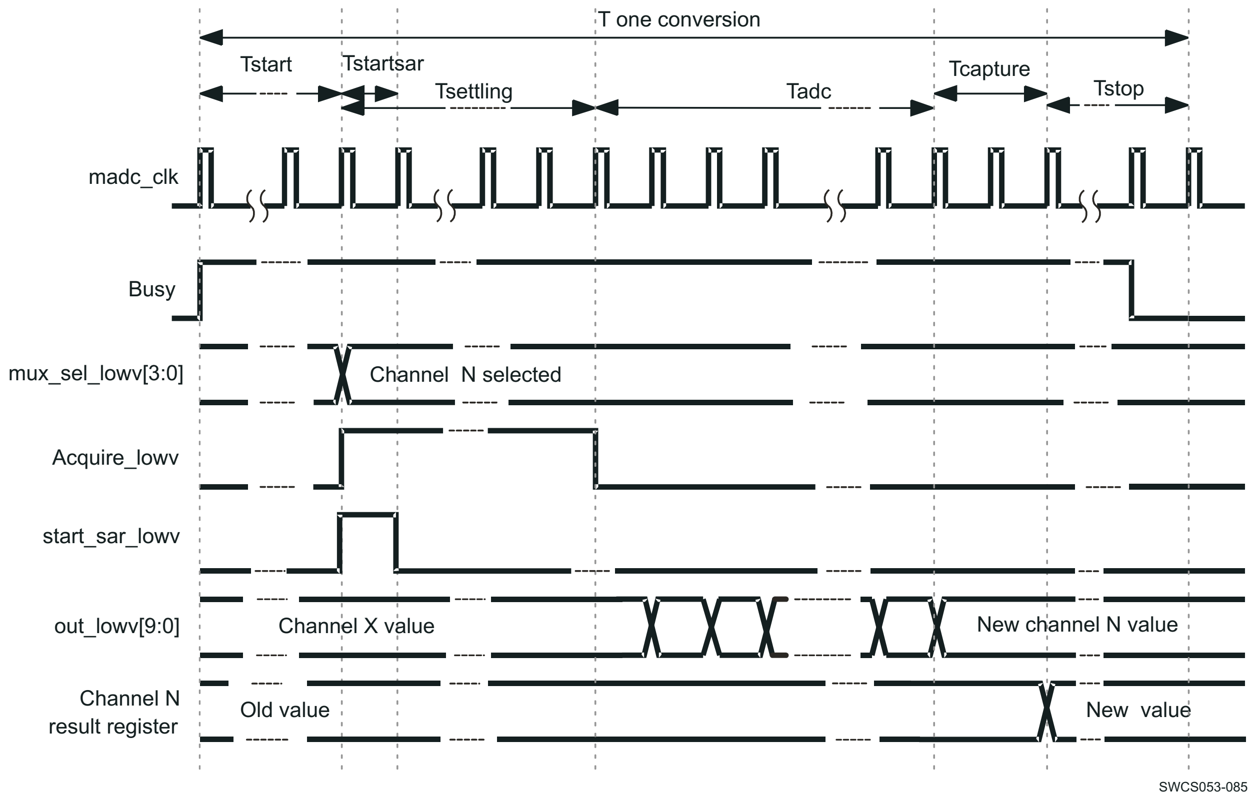


Figure 9-1. One Conversion Sequence General Timing Diagram

9.4 Power Consumption

Table 9-4. Power Consumption

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power on consumption	Running frequency f = 1 MHz	0.85	1 (1)	1.15	mA
Power down consumption		0.85	1	1.15	µA

(1) The consumption is given in stand-alone mode.

10 LED Drivers

10.1 General Description

Two arrays of parallel LEDs are driven (dedicated for the phone light). The parallel LEDs are supplied by VBAT and the external resistor value is given for each of them. The TPS65951 supports two open-drain LED drivers for keypad backlight, having drain connections tolerant of the main battery voltage.

Figure 10-1 shows the LED driver block diagram. Table 10-1 summarizes the LED driver electrical characteristics.

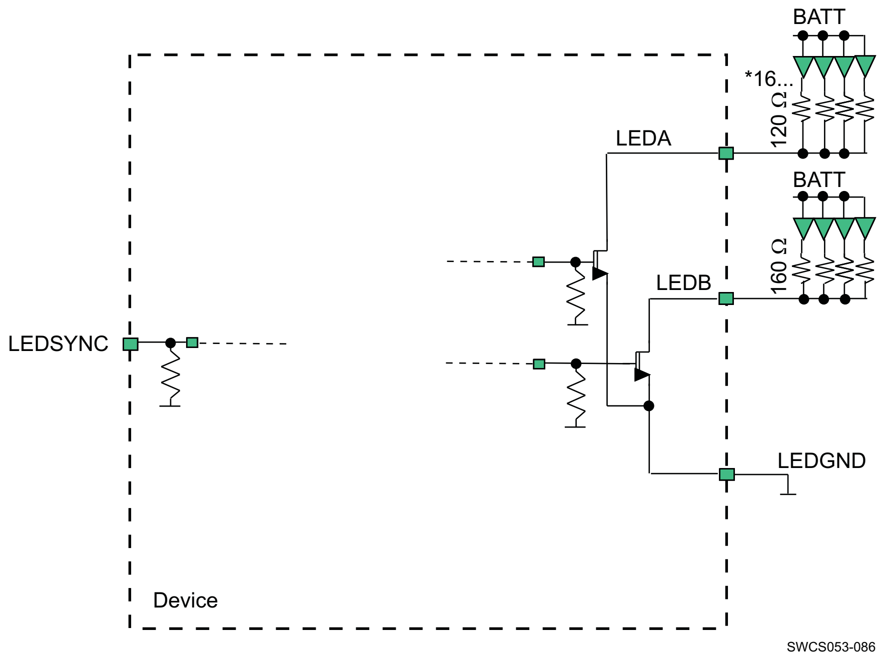


Figure 10-1. LED Driver Block Diagram

For the component values, see Table 12-1, *TPS65951 External Components*.

Table 10-1. Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
switch on resistance	I_O = 160 mA		3	4	Ω
	I_O = 60 mA		10	12	

11 Debouncing Time

Debounce times are listed in Table 11-1. Refer to Section 8 for BCI specific debounce times.

Table 11-1. Debouncing Time

DEBOUNCING FUNCTIONS	BLOCK	PROGRAMMABLE	DEBOUNCING TIME	DEFAULT
Main battery charged threshold	Battery monitoring	No	580 µs	580 µs
Main battery low threshold detection		No	60 µs	60 µs
Main battery plug detection (with charger connected)		No	60 µs	60 µs
Debouncing functions interrupt generation debounce for charger plug	POWER	No	125.6 µs	125.6 µs
Plug/unplug detection VBUS(1)	USB	Yes	0 to 250 ms	30 ms
Plug/unplug detection ID(2)	USB	Yes	0 to 250 ms	50 ms
Debouncing functions interrupt generation debounce for VUSB and ID(3)	POWER	Yes	0 to 233 ms	233 ms
Hot-die detection	Thermistor	No	60 µs	60 µs
Thermal shutdown detection		No	60 µs	60 µs
PWRON(4)	Start/stop button	No	31.25 ms	31.25 ms
NRESWARM	Button reset	No	60 µs	60 µs
Headset detection (plug/unplug)	GPIO	Yes	0 or 28 ms ± 2 ms	0 ms
MMC1/2 (plug/unplug)	GPIO	Yes	0 or 28 ms ± 2 ms	0 ms

(1) Programmable in the VBUS_DEBOUNCE register.
(2) Programmable in the ID_DEBOUNCE register.
(3) Programmable in the RESERVED_E[2:0] CFG_VBUSDEB register
(4) The PWRON signal is debounced 1024 × CLK32K (maximum 1026 × CLK32K) falling edge in master mode.

When a switch/button is connected to the PWRON pad then this can be used as a means to power-on and power-off the device. A short press generating a negative pulse will transition the phone from WAIT-ON (OFF) state to ACTIVE state. A long press of 8 seconds will transition the device to WAIT-ON (OFF) state.

12 External Components

Table 12-1. TPS65951 External Components

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
POWER SUPPLIES					
VDD1	Capacitor	$C_{VDD1.IN}$	10 μF	Range ± 50% ESR min = 1 mΩ ESR max = 20 mΩ Taiyo Yuden: JMK212BJ106KD	Figure 6-1
	Capacitor	$C_{VDD1.OUT}$	10 μF (1)	Range ± 50% ESR min = 1 mΩ ESR max = 20 mΩ Taiyo Yuden: JMK212BJ106KD	
	Inductor	L_{VDD1}	1 μH	Range ± 30% DCR max = 100 mΩ	
VDD2	Capacitor	$C_{VDD2.IN}$	10 μF	Range ± 50% ESR min = 1 mΩ ESR max = 20 mΩ Taiyo Yuden: JMK212BJ106KD	Figure 6-1
	Capacitor	$C_{VDD2.OUT}$	10 μF	Range ± 50% ESR min = 1 mΩ ESR max = 20 mΩ Taiyo Yuden: JMK212BJ106KD	
	Inductor	L_{VDD2}	1 μH	Range ± 30% DCR max = 100 mΩ	
VIO	Capacitor	$C_{VIO.IN}$	10 μF	Range ± 50% ESR min = 1 mΩ ESR max = 20 mΩ Taiyo Yuden: JMK212BJ106KD	Figure 6-1
	Capacitor	$C_{VIO.OUT}$	10 μF	Range ± 50% ESR min = 1 mΩ ESR max = 20 mΩ Taiyo Yuden: JMK212BJ106KD	
	Inductor	L_{VVIO}	1 μH	Range ± 30% DCR max = 100 mΩ	
VUSB3V1	Capacitor	$C_{VUSB.3P1}$	2.2 μF	Range: 0.5 μF to 2.7 μF ESR min = 20 mΩ ESR max = 300 mΩ	Figure 6-1 Figure 7-2
VUSB1V5	Capacitor	$C_{VINTUSB1P5.OUT}$	2.2 μF	Range: 0.5 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1 Figure 7-2
VUSB1V8	Capacitor	$C_{VINTUSB1P8.OUT}$	2.2 μF	Range: 0.5 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1 Figure 7-2
VDAC	Capacitor	$C_{VDAC.IN}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
	Capacitor	$C_{VDAC.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	
VPLLA3R	Capacitor	$C_{VPLLA3R.IN}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VPLL1	Capacitor	$C_{VPLL1.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VPLL2	Capacitor	$C_{VPLL2.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1

(1) Refer to application note *Using Power IC for OMAP 34xx to 36xx Family*, SWCA096.

Table 12-1. TPS65951 External Components (continued)

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
VMMC1	Capacitor	$C_{VMMC1.IN}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
	Capacitor	$C_{VMMC1.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	
VMMC2	Capacitor	$C_{VMMC2.IN}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
	Capacitor	$C_{VMMC2.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	
VAUX12S	Capacitor	$C_{VAUX12S.IN}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VAUX1	Capacitor	$C_{VAUX1.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VAUX2	Capacitor	$C_{VAUX2.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VAUX3	Capacitor	$C_{VAUX3.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VAUX4	Capacitor	$C_{VAUX4.IN}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
	Capacitor	$C_{VAUX4.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	
VINT	Capacitor	$C_{VINT.IN}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VINTANA1	Capacitor	$C_{VINTANA1.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VINTANA2	Capacitor	$C_{VINTANA2.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VINTDIG	Capacitor	$C_{VINTDIG.OUT}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 6-1
VBAT.USB	Capacitor	$C_{VBAT.USB}$	1 μF	Range: 0.3 μF to 2.7 μF ESR min = 20 mΩ ESR max = 600 mΩ	Figure 7-2
USB CP	Capacitor	$C_{VBUS.FC}$	2.2 μF	Range ± 40% ESR max = 20 mΩ	Figure 7-2
	Capacitor	$C_{VBUS.IN}$	10 μF	Range ± 50%	
	Capacitor	C_{CPOUT}	4.7 μF	Range ± 40% ESR max = 20 mΩ	

Table 12-1. TPS65951 External Components (continued)

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
			USB		
VBUS	Capacitor	C_{VBUS}	4.7 µF	Range ± 40% ESR max = 20 mΩ	Figure 7-2
			32.768 kHz		
	Capacitor	C_{XIN}	10 pF	Range: 9 pF to 12.5 pF	Figure 4-6
	Capacitor	C_{XOUT}	10 pF	Range: 9 pF to 12.5 pF	
	Quartz	$X_{32.768kHz}$	32.768 kHz	±30 ppm (at 25°C) ±200 ppm (–40°C to 85°C)	
			AUDIO		
Earpiece	Capacitor	C_{EAR}	100 pF	Range: 0 to 100 pF	Figure 5-3
8-Ω Hands-free Right	Ferrite bead	$L_{HFR.M}$		NEC: N2012ZPS121T50 TDK: MPZ1608S221A Taiyo Yuden:BKP1608HS271	Figure 5-6
	Ferrite bead	$L_{HFR.P}$		NEC: N2012ZPS121T50 TDK: MPZ1608S221A Taiyo Yuden:BKP1608HS271	
	Capacitor	C_{HFR}	1 µF		
	Capacitor	$C_{HFR.M}$	1 nF		
	Capacitor	$C_{HFR.P}$	1 nF		
8-Ω Hands-free Left	Ferrite bead	$L_{HFL.M}$		NEC: N2012ZPS121T50 TDK: MPZ1608S221A Taiyo Yuden:BKP1608HS271	Figure 5-6
	Ferrite bead	$L_{HFL.P}$		NEC: N2012ZPS121T50 TDK: MPZ1608S221A Taiyo Yuden:BKP1608HS271	
	Capacitor	C_{HFL}	1 µF		
	Capacitor	$C_{HFL.M}$	1 nF		
	Capacitor	$C_{HFL.P}$	1 nF		
Headset Left	Capacitor	C_S	22 µF/ 47 µF		Figure 5-10 through Figure 5-13
	Resistor	R_S	0 to 33 Ω		
	Capacitor	C_I	47 pF		
Headset Right	Capacitor	C_S	22 µF/ 47 µF		Figure 5-10 through Figure 5-13
	Resistor	R_S	0 to 33 Ω		
	Capacitor	C_I	47 pF		
Headset Mic	Capacitor	$C_{HM.M}$	100 nF		Figure 5-10 through Figure 5-13
	Capacitor	$C_{HM.P}$	100 nF		
	Capacitor	$C_{HM.O}$	47 pF		
	Resistor	$R_B + R_{SB}$	2.2 kΩ/ 2.7 kΩ		
	Capacitor	C_B	0 to 200 pF	If greater than 200 pF, then it needs a serial resistor for bias stability	
External Class D Predriver Left	Capacitor	$C_{PL.O}$	50 pF		Figure 5-15
	Capacitor	C_{PL}	1 µF		
	Resistor	R_{PL}	> 15 kΩ		
	Resistor	$R_{PL.M}$	> 15 kΩ		
	Resistor	$R_{PL.O}$	10 kΩ	See note in Figure 5-15 (impact on gain accuracy)	
	Capacitor	$C_{PL.M}$	1 µF		

Table 12-1. TPS65951 External Components (continued)

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
External Class D Predriver Right	Capacitor	$C_{PR.O}$	50 pF		Figure 5-15
	Capacitor	C_{PR}	1 µF		
	Resistor	R_{PR}	> 15 kΩ		
	Resistor	$R_{PR.M}$	> 15 kΩ		
	Resistor	$R_{PR.O}$	10 kΩ	ee note in Figure 5-15 (impact on gain accuracy)	
	Capacitor	$C_{PR.M}$	1 µF		
Vibra H-Bridge	Ferrite Bead	$L_{V.M}$		BLM18BD221S1N	Figure 5-16
	Ferrite Bead	$L_{V.P}$		BLM18BD221S1N	
	Capacitor	$C_{V.V}$	1 µF		
	Capacitor	$C_{V.M}$	1 nF		
	Capacitor	$C_{V.P}$	1 nF		
MIC Main (pseudo differential mode)	Capacitor	$C_{MM.M}$	100 nF		Figure 5-22
	Capacitor	$C_{MM.P}$	100 nF		
	Capacitor	$C_{MM.O}$	47 pF		
	Resistor	$R_{MM.O}$	500 Ω		
	Resistor	$R_{MM.MP}$	1.7 kΩ		
	Capacitor	$C_{MM.B}$	0 to 200 pF	If greater than 200 pF, then it needs a serial resistor for bias stability	
MIC Sub (pseudo differential mode)	Capacitor	$C_{MS.M}$	100 nF		Figure 5-22
	Capacitor	$C_{MS.P}$	100 nF		
	Capacitor	$C_{MS.O}$	47 pF		
	Resistor	$R_{MS.O}$	500 Ω		
	Resistor	$R_{MS.MP}$	1.7 kΩ		
	Capacitor	$C_{MS.B}$	0 to 200 pF	If greater than 200 pF, then it needs a serial resistor for bias stability	
MIC Main (differential mode)	Capacitor	$C_{MM.M}$	100 nF		Figure 5-23
	Capacitor	$C_{MM.P}$	100 nF		
	Capacitor	$C_{MM.PM}$	47 pF		
	Capacitor	$C_{MM.O}$	47 pF		
	Capacitor	$C_{MM.GM}$	47 pF		
	Capacitor	$C_{MM.GP}$	47 pF		
	Resistor	$R_{MM.BP}$	1 kΩ		
	Resistor	$R_{MM.GM}$	1 kΩ		
	Capacitor	$C_{MM.B}$	0 to 200 pF	If greater than 200 pF, then it needs a serial resistor for bias stability	
MIC Sub (differential mode)	Capacitor	$C_{MS.M}$	100 nF		Figure 5-23
	Capacitor	$C_{MS.P}$	100 nF		
	Capacitor	$C_{MS.PM}$	47 pF		
	Capacitor	$C_{MS.O}$	47 pF		
	Capacitor	$C_{MS.GM}$	47 pF	When MIC Sub not used, capacitor is not needed and node can be connected to ground (preferred) or be left floating.	
	Capacitor	$C_{MS.GP}$	47 pF		
	Resistor	$R_{MS.BP}$	1 kΩ		
	Resistor	$R_{MS.GM}$	1 kΩ		
	Capacitor	$C_{MS.B}$	0 to 200 pF	If greater than 200 pF, then it needs a serial resistor for bias stability	

Table 12-1. TPS65951 External Components (continued)

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
VMIC1	Capacitor	$C_{VMIC1.OUT}$	1 µF	Range: 0.3 µF to 3.3 µF ESR min = 20 mΩ ESR max = 600 mΩ	
VMIC2	Capacitor	$C_{VMIC2.OUT}$	1 µF	Range: 0.3 µF to 3.3 µF ESR min = 20 mΩ ESR max = 600 mΩ	
Silicon MIC	Capacitor	C_{SM}	1 µF		Figure 5-26
	Capacitor	$C_{SM.P}$	100 nF		
	Capacitor	$C_{SM.M}$	100 nF	When Silicon MIC not used, capacitor is not needed and node can be connected to ground (preferred) or be left floating.	
	Capacitor	$C_{SM.PG}$	47 nF		
	Resistor	R_{SM}	> 500 Ω		
Auxiliary Left	Capacitor	C_{AUXL}	100 nF		Figure 5-27
	Capacitor	$C_{AUXL.M}$	47 pF	When not used, capacitor is not needed.	
Auxiliary Right	Capacitor	C_{AUXR}	100 nF		
	Capacitor	$C_{AUXR.M}$	47 pF	When not used, capacitor is not needed.	
LED DRIVER					
	Resistor	$R_{LED.A}$	120 Ω	Range ± 5% (needed for each LED)	Figure 10-1
	Resistor	$R_{LED.B}$	160 Ω	Range ± 5% (needed for each LED)	
BATTERY CHARGER					
VPRECH	Capacitor	C_{PRECH}	1 µF		
VBAT	Capacitor	C_{CV}	80 µF		
I^2C BUS - EXTERNAL PULLUP					
I^2C SmartReflex	Resistor	$R_{PSR.SDA}$	If C_{PCB} is less than 12 pF, there is no need for an external pullup resistor. If C_{PCB} is greater than 12 pF, the external pullup resistors are: • for C_B = 50 pF, the pullup resistor is 940 Ω • for C_B = 100 pF, the pullup resistor is 470 Ω Ensure that the internal pullup value is: R = 3 kΩ ±30%		Section 7.4
	Resistor	$R_{PSR.SCL}$			
I^2C Control	Resistor	$R_{CNTL.SDA}$			
	Resistor	$R_{CNTL.SCL}$			

13 TPS65951 Package

13.1 TPS65951 Standard Package Symbolization

Table 13-1. TPS65951 Nomenclature Description

FIELDS	MEANING
P	Marking used to note prototype (X), preproduction (P), or qualified/production device (Blank)(1)
A	Mask set version descriptor (initial silicon = BLANK, first silicon revision = A, second silicon revision = B,...)(2)
YM	Year month
LLLLS	Lot code
$	Fab Planning Code

(1) BLANK in the symbol or part number are collapsed so there are no gaps between characters.
(2) Initial silicon version is ES1.0; first revision can be named ES2.0, ES1.1 or ES1.01 depending on the level of change.
NOTE: Device name maximum 10 characters.

13.2 Package Thermal Resistance Characteristics

Table 13-2 provides the thermal resistance characteristics for the recommended package types used on the TPS65951 devices.

Table 13-2. TPS65951 Thermal Resistance Characteristics

PACKAGE	$R_{\theta JA}$(°C/W)	$R_{\theta JB}$(°C/W)	$R_{\theta JC}$(°C/W)	BOARD TYPE
TPS65951	36	22	11(1)	2S2P(2)

(1) Not applicable since the POP package has a memory package on top, no heat sink can be used.
(2) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Area Array Surface Mount Package Thermal Measurements).

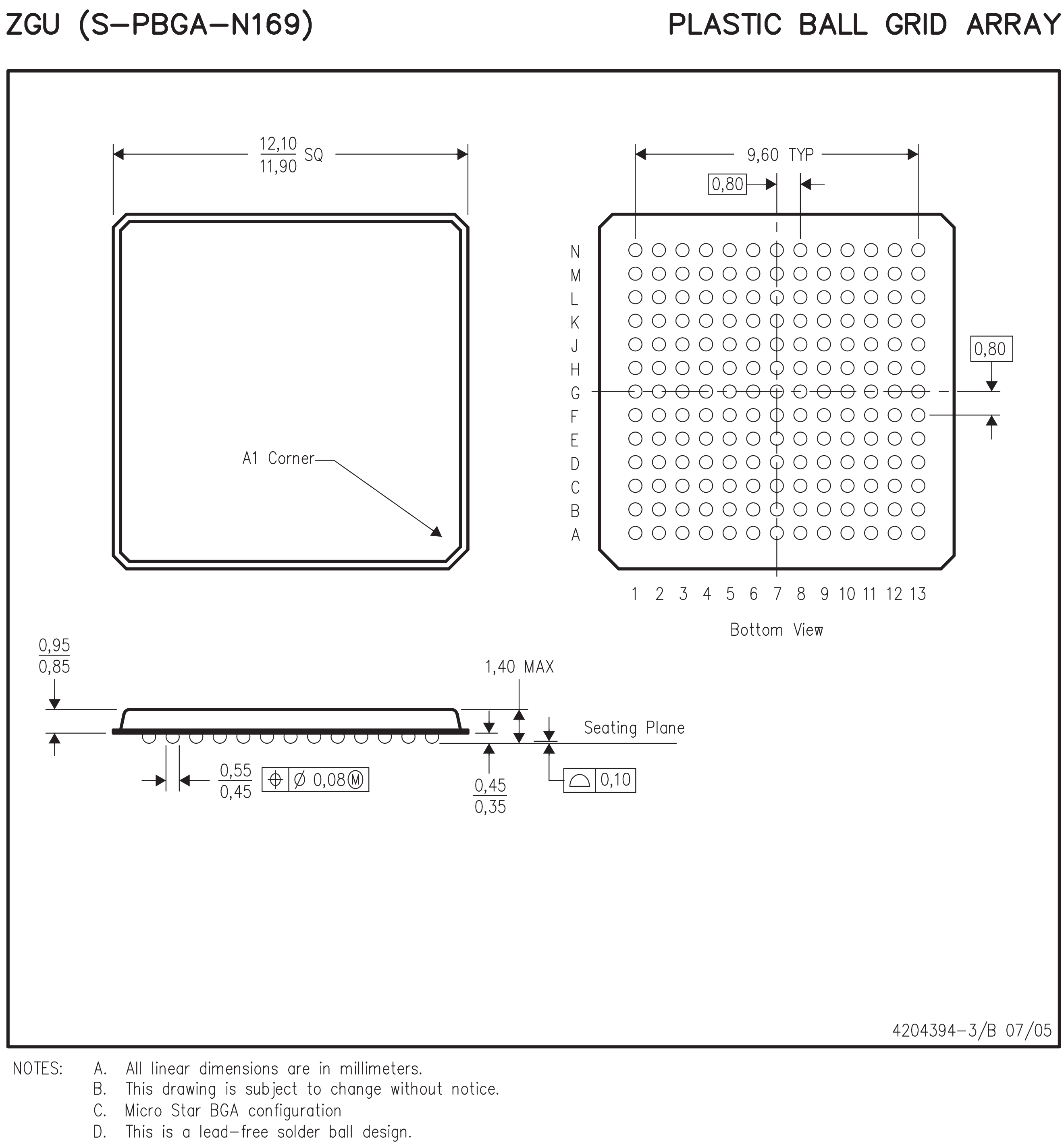
13.3 Packaging Information

Table 13-3. Orderable Parts

Orderable Device	Package Type	Package Drawing	Pins	Package Quantity	Eco Plan
PTPS65951A1ZGU	BGA MICROSTAR	ZGU	169	250	Green (RoHS & no Sb/Br)
PTPS65951A1ZGUR	BGA MICROSTAR	ZGU	169	2500	Green (RoHS & no Sb/Br)

13.4 Mechanical Data

Figure 13-1 shows the TPS65951 mechanical package.



SWCS053-090

Figure 13-1. TPS65951 Mechanical Package

14 Glossary

ADC	Analog-to-Digital Converter
ALC	Automatic Level Control
ASIC	Application-Specific Integrated Circuit
BCI	Battery Charger Interface
BGA	Ball Grid Array
BW	Signal Bandwidth
CMOS	Complimentary Metal Oxide Semiconductor
CMT	Cellular Mobile Telephone
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DBB	Digital Baseband
DM	Data Manual
DSP	Digital Signal Processor
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FSR	Full-Scale Range
GP	General-purpose
GPIO	General-purpose Input Output
hiZ	High-Impedance
HS	High Speed or High Secure
HW	Hardware
I^2C	Inter Integrated Circuit
I2S	Inter IC Sound
IC	Integrated Circuit
ICN	Idle Channel Noise
ID	Identification
IDDQ	Direct Drain Quiescent Current
IF	Interface
IO or I/O	Input/Output
JTAG	Joint Test Action Group, IEEE 1149.1 standard
LED	Light emitting diode
LDO	Low Dropout Regulator
LJF	Left-Justified Format
LS	Low speed
MADC	Monitoring Analog-to-Digital Converter
MCPC	Mobile Computing Promotion Consortium
NA	Not Applicable
OCP	Open Core Protocol
OTG	On the Go

PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Pulldown
PDM	Pulse Density Modulated
PFM	Pulse Frequency Modulation
PLL	Phase Locked Loop
POL	Polarity
PSRR	Power Supply Rejection Ratio
PU	Pullup
PWL	Pulse Width Length
PWT	Pulse Width Time
PWM	Pulse Width Modulation
RJF	Right-Justified Format
RTC	Real-Time Clock
RX	Receive
SDI	Serial Display Interface
SMPS	Switch-Mode Power Supplies
SNR	Signal-to-Noise Ratio
SW	Software
SYNC/SYNCHRO	Synchronization
SYS	System
TBD	To be defined
THRU	feed through
TRM	Technical Reference Manual
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
ULPI	UTMI+ Low Pin Interface
UPR	Uninterrupted Power Rail
USB	Universal Serial Bus
UTMI	USB transceiver Macrocell Interface

14.1 Revision History

The following table summarizes the TPS65951 Data Manual versions.

Note: Numbering may vary from previous versions.

Version	Literature Number	Date	Notes
F	SWCS053F	May 2012	See [1]

(1) TPS65951 Data Manual, (SWCS053F) - update Table 2-3; Change ball number of VINTUSB1P8 from N7 to M7.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65951A1ZGU	ACTIVE	BGA MICROSTAR	ZGU	169	1	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TPS65951A1ZGUR	ACTIVE	BGA MICROSTAR	ZGU	169	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

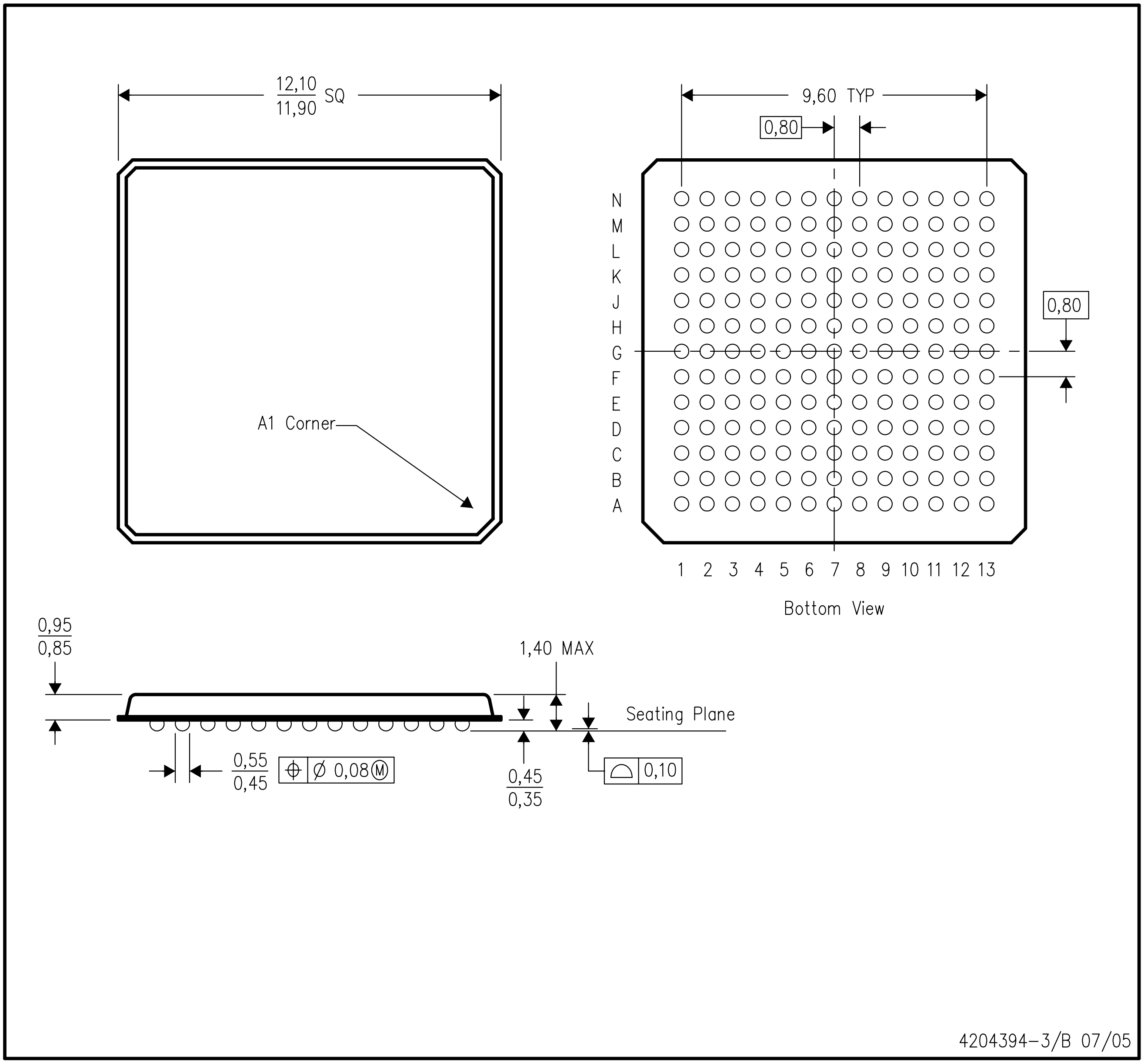
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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ZGU (S–PBGA–N169) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Micro Star BGA configuration
D. This is a lead–free solder ball design.

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